USER NOTES

July 25, 1986 984-1007-002

The following information is provided to supplement the UniPak Manual. This document provides instructions for updating the UniPak Manual so that it reflects the latest UniPak equipment update. Provided below is a list of the configuration numbers for the latest equipment configuration which the updated manual covers. Also provided are the new replacement pages to be inserted into the manual, instructions for inserting those pages into the manual, and a note on timing diagrams and schematics.

The numbers listed in the table below are part numbers and version numbers used by Data I/O to identify the configuration of the documentation and equipment you have purchased. Columns two and three show the configuration of the equipment shipped to you. Column one shows the configuration of the manual that was shipped with your equipment.

THIS USER NOTE APPLIES TO:

Manual Part No.	Model No.	Version No.
981-0003-001 and up	UniPak	V11

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UNIPAK

Firmware Update Kit

985-0007-002 JULY 86

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Applies to Engineering Part Number 950-0099-011 and up.
Text pages 090-0258-002.

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INTRODUCTION

WARNING

The instructions contained in this document are for qualified service personnel only. Do not attempt to perform them unless you are qualified to do so.

This kit contains the hardware and instructions necessary to update your UniPak. The parts included in the update kit are listed in Table 1:

Table 1. 953-0007-011 Update Kit V11 Firmware

Description	Quantity	Location	Data I/O Part No.
EPROM	1	U1	324-0003-028
EPROM	1	U2	324-0003-029
EPROM	1	U3	324-0003-030
EPROM	1	U4	324-0003-031
Decode PROM	1	U8	324-0003-019
Label	1	--	--

Firmware Configuration/Version Number: AA8F/11

CAUTION

The firmware update components are static sensitive. Observe the standard handling precautions, otherwise, damage to the component(s) may result.

UNIPAK UPDATE KIT INSTALLATION

The following paragraphs describe how to install the update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size)
- One slot-head screwdriver (medium size)
- IC extractor tool, or small slot-head screwdriver
- Soldering equipment

UniPak Disassembly

To disassemble the UniPak, refer to figures 1 through 3 and follow the procedures listed below.

1. Remove the UniPak from the programmer.
2. Set the UniPak face down on the flat surface of a static-free work station.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners until they hang loosely; the fasteners will not separate from their standoffs (see figure 1a).
4. Lift the card cage up slightly, then pull it out (as shown in figure 1b) to unlock the flanges.

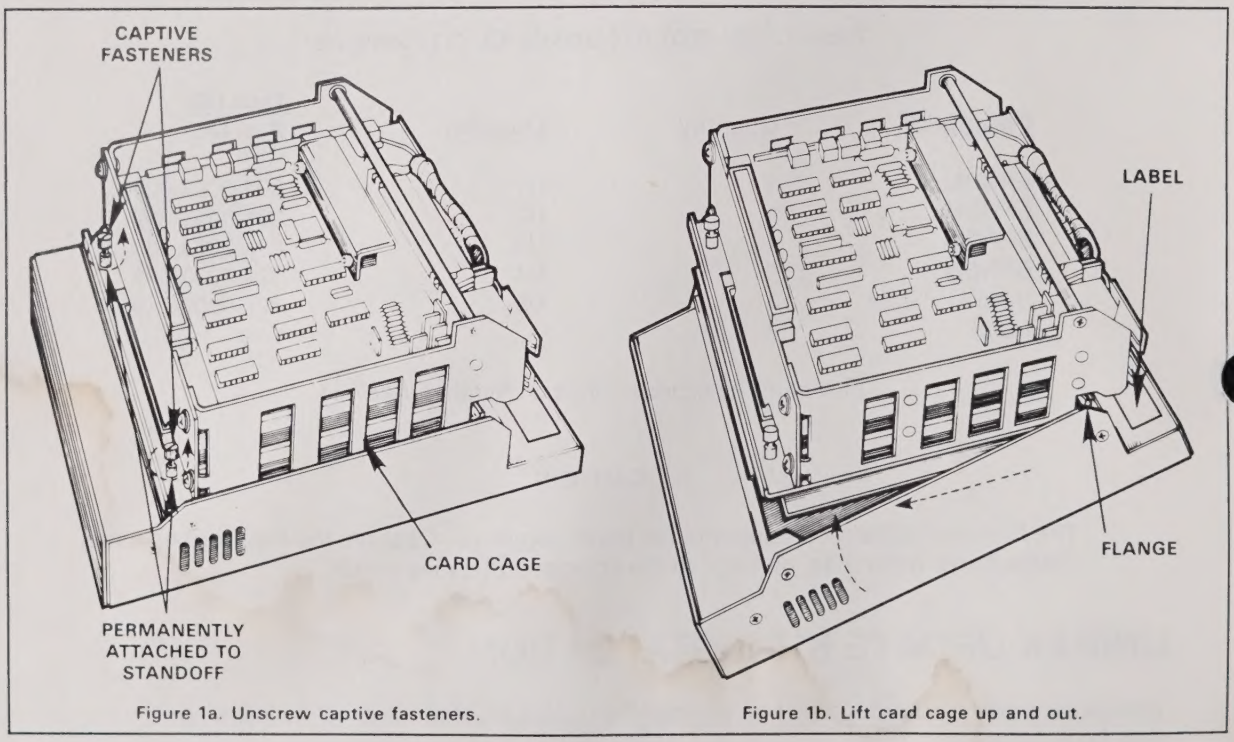

Figure 1a. Unscrew captive fasteners.

Figure 1b. Lift card cage up and out.

Figure 1. UniPak Disassembly

5. Lift the card cage up and out of the top cover until you can see the socketboard interconnect cable (see figure 2). Do not detach the interconnect cable.

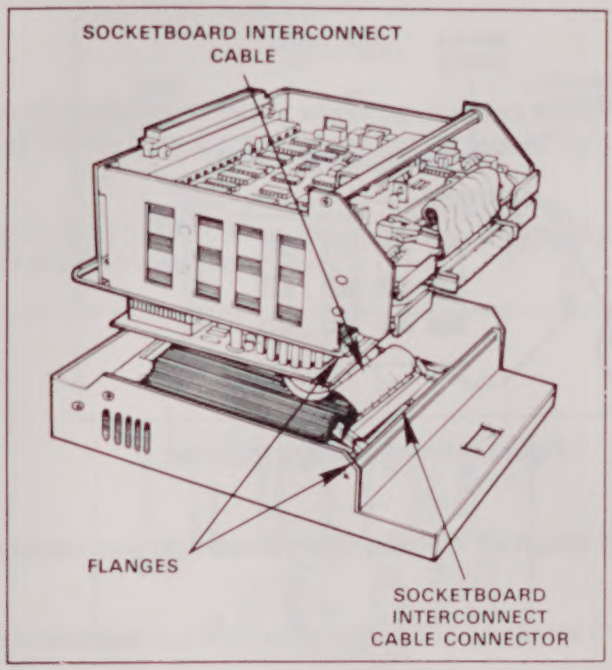

Figure 2. Card Cage Separation from Top Cover

6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see figure 3). Retain the washers and screws for reassembly.

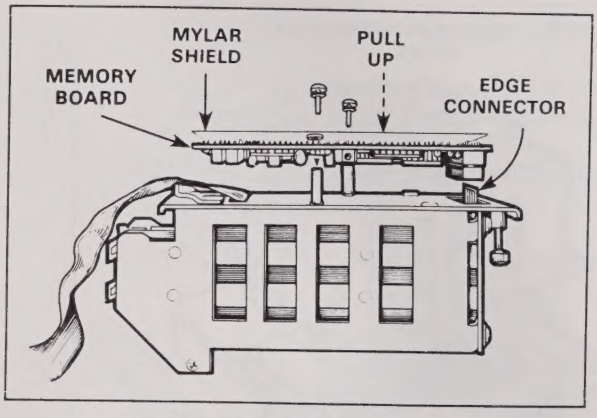

Figure 3. Memory Board Removal

8. Pull the memory board straight up to unplug it from the card edge connector (as shown in figure 3).

9. Turn the memory board over so the component side faces up in preparation for update firmware installation.

Update Kit Firmware Installation

The following steps describe how to install the components of the update kit into your UniPak. Follow the procedures in the order that they are presented here.

CAUTION

The update kit components are static sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the component(s).

1. Remove EPROMs U1, U2, U3, and U4 from the memory board (shown in figure 4) using the IC extractor tool, or the small slot-head screwdriver.

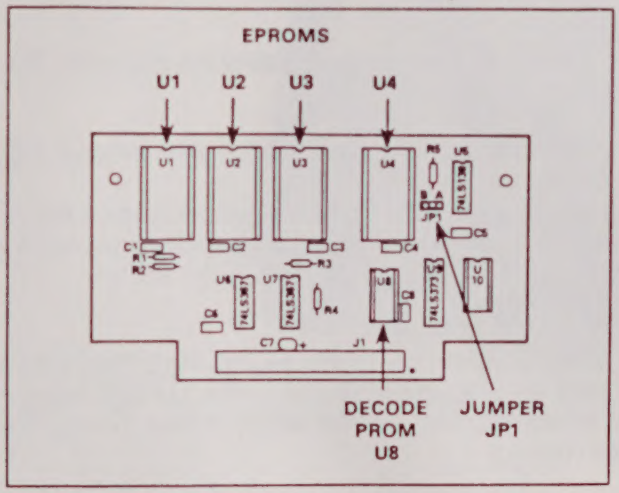

Figure 4. Update Component Location

2. Observe the position of wire strap jumper JP1 (shown in figure 4). If the wire strap jumper JP1 is located in position A, perform steps 3 through 5 which follow. If the jumper is located in position B, proceed directly to step 6 (bypassing steps 3 through 5).

3. If jumper JP1 is in position A, remove Decode PROM U8 using the extractor tools.

4. After removing Decode PROM U8, unsolder jumper JP1 from position A and resolder it in position B.

5. Install the update kit Decode PROM U8 in memory board socket U8. Refer to table 1 for update kit component part numbers.

6. Install the update kit EPROMs U1, U2, U3, and U4 in memory board sockets U1, U2, U3, and U4, respectively. Refer to table 1 for update kit component part numbers.

UniPak Reassembly

Reassemble the UniPak by referring to figures 1 through 3 and following the steps listed below.

1. Plug the memory board into its card edge connector until it is firmly seated (see figure 3).

2. Replace the armite or mylar shield, washers, and two Phillips-head screws.

3. Replace the card cage, containing the memory board, by turning it over so that the memory board faces into the UniPak top cover. Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (see figures 2 and 1b). Then gently set the card cage back into the top cover.

4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.

5. Affix the label enclosed in the update kit on the back side of the top cover. The label location is shown in figure 1b.

6. Perform a self-test on the UniPak by installing it in a programmer and applying power.

   If the programmer fails to power-up correctly, or the self-test message is not displayed, check to make sure that all of the update kit installation procedures were performed correctly. Attempt the self-test again. If the self-test still fails, contact your local Data I/O Service Center.

7. Verify correct firmware configuration/version number by entering **SELECT E F START** from the programmer keys. Check the programmer display for the four-digit configuration number and the two-digit version number. See the bottom of table 1 on the first page of this document for these numbers.

   If the configuration and version numbers shown in table 1 are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. If the configuration and version numbers still do not match those shown in table 1, contact your local Data I/O Service Center.

   If the configuration and version numbers shown in table 1 are displayed, then the update kit firmware installation is complete.

UniPak™

981-0003-002

JULY 86

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Data I/O reserves the right to make changes to this document without notice at any time.

NOTE

This configuration of the UniPak™ varies from previous configurations in that it uses some hexadecimal family codes. Some decimal family numbers have been changed. While this configuration will work with any Data I/O Universal Programmer (see section 1.1), to use hexadecimal families it may be necessary to update your programmer. Refer to section 1.2 of this manual for maintenance compatibility requirements. Model 1730s cannot handle hexadecimal families at this time. Some of the new larger devices will require that the programmer RAM be expanded. Consult your nearest Data I/O representative for update availability.

Applies to: Engineering Part No. 950-0099-011 and up
Text Part Number 090-0064-002

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008-1998	Address Card
008-1999	Motherboard
30-701-7997	Waveform Generator
30-702-0045	UniPak™ Memory
30-702-7995	Socket Assembly

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SECTION 1
INTRODUCTION

1.1 OVERVIEW

Data I/O's UniPak™ reliably programs over 400 popular MOS and bipolar devices. Values for programming variables, including pinouts, voltage levels and timing, are stored in firmware tables. When you choose the family and pinout codes for a particular device, the programmer uses information in these tables to assemble a specialized programming routine in scratch RAM. This method allows high-speed operation with minimum firmware overhead. The UniPak™ is designed to adapt to the programming requirements of many different devices. Pinout variations are handled by seven device sockets on the UniPak™ and, in some cases, by adapters which connect to socket 1 or 2. Specially designed electronic switches allow programming of both bipolar and MOS devices.

To maximize control speed during programming, the UniPak™ makes extensive use of addressable latches for control signals. For flexibility in waveform generation, digital-to-analog converters (DACs) control all major power supplies, with several rise and fall times selected by firmware.

1.2 PROGRAMMER COMPATIBILITY

Before using the -011 version of the UniPak™, read the information in this section to be sure your programmer does not require a modification. Either or both of two modifications to your System 17 or 19 may be required for compatibility with the -007 or later version of the UniPak™:

A. It may be necessary to make a small hardware modification to the System 17/19 Controller (702-1520).

B. A firmware update may be necessary.

29A Universal Programmers and 100A Production Programmers may need firmware updates.

1.2.1 Hardware Modification

System 19s with serial numbers below 1516 and System 17s with serial numbers below 219 will require small modifications for use with the UniPak™. The UniPak™ may cause error messages which are invalid if the modification is not made. No other programmer functions are affected, nor will attempting an operation harm the programmer, the UniPak™, or a device in the socket.

CAUTION

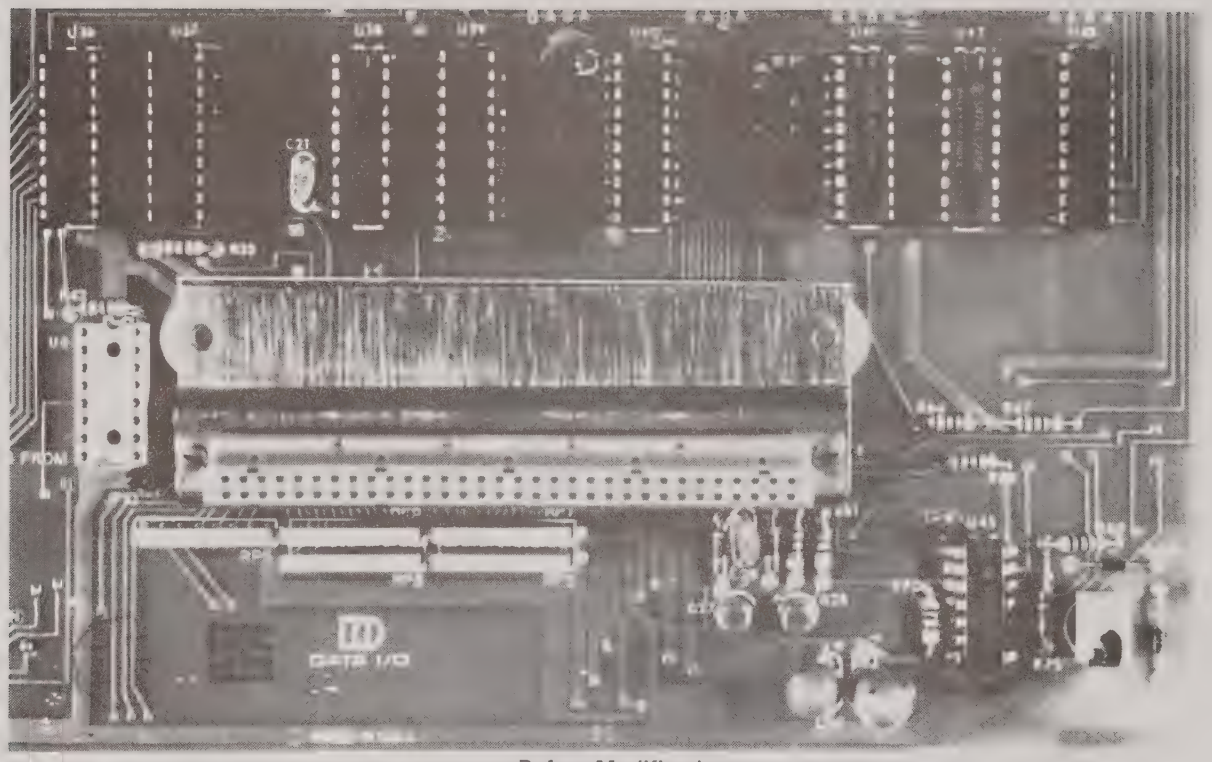
The following hardware modification to the System 17 and 19 should be performed by a qualified technician only. If the facilities are not available to perform the modification, contact your local Data I/O Service Center. A list of all Data I/O service centers is located in the back of this manual.

Modification Instructions

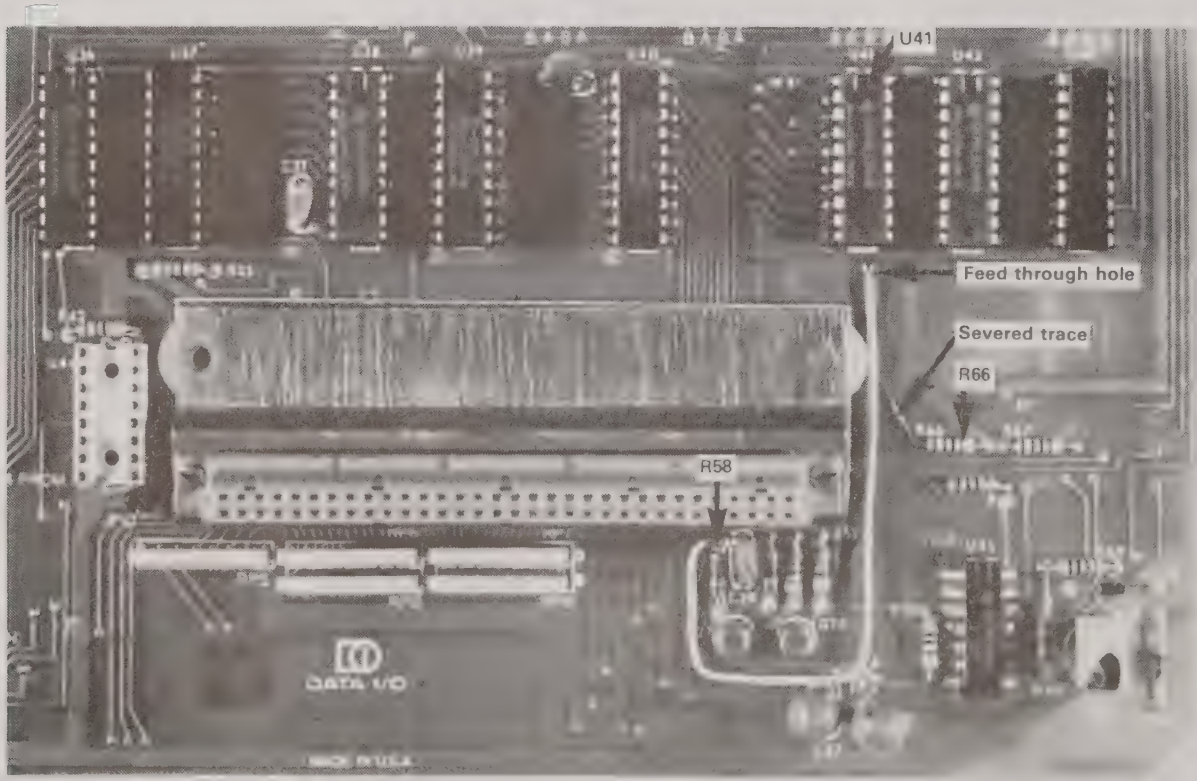
1. Unplug power cord.
2. Remove Programming Pak.
3. Remove protection shield.
   a. Pull the two snap-lock connectors and lift them gently.
   b. Lift the back edge of the plate first and pull it up slightly and turn it to the left until it is clear.
4. Remove top cover.
   a. Turn the programmer on its top.
   b. Remove the four cover screws.
   c. Turn the programmer upright and lift the cover off.
5. Remove display panel.
   a. Remove four screws located at the corner of the display panel.
   b. Remove the screw fastening the support bracket to the power supply assembly.
   c. Remove the screw fastening the support bracket to the front of the base.
   d. If there is a screw fastening the support bracket to the bottom plate, remove it.
6. Refer to figure 1-1. Sever the trace connecting R66 to U41 pin 1 just above R66 (left side).
7. Install an insulated wire from the top side of R58 (just *left* of C29, in front of the Programming Pak connector) to U41 pin 1. To connect to U41 pin 1, use the feed-through hole on the trace tying R66 to U41. (See figure 1.)
8. Reinstall the display panel top cover and protective shield by reversing the removal procedures.

Programmer Check

9. Install a Programming Pak.
   a. Check the programmer for proper initialization.
   b. Load a device with a known data pattern and perform a verify to confirm proper operation.



a. Before Modification



b. After Modification

Note: Your controller may appear slightly different. Be sure connections are made to the components designated in this bulletin.

Figure 1-1. Jumper-Wire Location on Programmer Controller, 702-1520

1.2.2 Software Update

Some programmers require a software update for compatibility with the -004 or later version of the UniPak™. Table 1-1 shows the revisions and software configuration-check numbers for each programmer configuration requiring a software update. If your System 17, 19, 29A or 100A is one of these revisions, contact a Data I/O sales representative to order the appropriate update kit.

To determine the revision level of a programmer, follow the procedure below to display the software configuration-check number and compare it to table 1-1.

- **System 19 and 29A, all configurations**: Key in Select Code B2-START.
- **System 29B, all configurations**: Key in Select Code B2-START. (All configurations are compatible.)
- **100A Production Programmer**: Key in Select Code 10.
- **System 1730**: Enter remote control and use the G command.
- **System 1731**: Enter remote control and use the CN command.

1.3 APPLICATIONS

Table A-1 lists all the devices that could be programmed with the UniPak™ when this manual was published. In many cases when a new device with industry standard pinout is introduced within a manufacturer's family, the UniPak™ WILL NOT require a revision to program it. For some new applications, such as to accommodate a new device family, a firmware update of the UniPak™ may be required. The revision number is stamped after the part number (950-0099) along the underside of the top edge of the UniPak™ socket assembly.

1.4 SPECIFICATIONS

The UniPak™ receives its power from the programmer mainframe. Programming waveforms are generated from raw programmer supplies using regulators controlled by the programmer's microprocessor. The controlling firmware is located on a circuit card within the UniPak™.

The physical and environmental specifications are:

- Altitude: Sea level to 3 km (10,000 ft.)
- Dimensions: 20.9 x 17.0 x 10.5 cm (8.2 x 6.7 x 4.2 in.)
- Humidity (operating): 90% maximum (noncondensing)
- Humidity (storage): 95% maximum (noncondensing)
- Temperature (operating): 0 to 40°C (32 to 104°F)
- Temperature (storage): −40 to 55°C (−40 to 131°F)
- Weight: 1.38 kg (3 lb. 0.5 oz.)

Table 1-1. Programmers Requiring Updates

System	Revision	Software Configuration Check Number
990 1900	A	F9CF
	B	00AC
	C	07CD
	D	0B11
	E	FC6A
	F	B16C
990 1901	A	89CC
	B	C089
	C	6BCD
990 1902	A	C56C
	B	8B82
	C	9141
	D	9002
	E	2068
	F	29CE
	G	3868
	H	3599
990 1903	A	2C23
	B	6A9B
	C	3A33
990 1730	A	6D7B
	B	ADF5
	C	35EE
	D	4180
	E	44F8
990 1731	A	93AA
	B	3A3A
29A	A	1ECA
	B	20A4
29A w/computer remote control	A	BB41
	B	C00B
100A	A	917F
	B	9405
	C	9DEE
	D	9BED

1.5 FIELD APPLICATIONS SUPPORT

Data I/O has field applications engineers (FAE's) throughout the world. They can provide additional information about interfacing Data I/O products with other equipment and answer questions about equipment. FAE's are located within the United States at the addresses listed in the back of this manual. For international applications support, contact your nearest Data I/O representative.

1.6 WARRANTY

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period of one year, unless specified otherwise, begins when you receive the equipment. The warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O service center.

1.7 SERVICE

Data I/O maintains service centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. This includes not only repairs, but also calibration of all Data I/O products. A list of all Data I/O service centers is located in the back of this manual.

1.8 ORDERING

To order equipment, contact your Data I/O sales representative. Orders must contain the following information:

- Description of the equipment (see the latest Data I/O price list or contact your sales representative for equipment and part numbers)
- Quantity of each item ordered
- Shipping and billing address of firm, including ZIP code
- Name of person ordering equipment
- Purchase order number
- Desired method of shipment

SECTION 2
INSTALLATION

2.1 INSPECTION

Your UniPak™ was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should, therefore, arrive free of any defect, without marks or scratches, and in perfect operating condition. However, carefully inspect the instrument for any damage that may have occurred in transit. If you note any damage, file a claim with the carrier and notify Data I/O.

2.2 UniPak™ INSTALLATION

The UniPak™ may be installed and removed with the programmer's power on; this feature allows you to retain data in RAM during module changes. If the programmer power is turned on before the UniPak™ is installed, you will hear a beep until the UniPak™ is installed.

NOTE

Voltage transients can cause device damage. Thus, be sure that all sockets are empty when:

- *switching power on or off*
- *installing or removing the UniPak™*

To install the UniPak™, do the following:

1. Slide the UniPak™ into the opening in the programmer (figure 2-1).
2. Tilt the UniPak™ up and gently push it back to hook the flange of the UniPak™ over the back edge of the programmer opening (figure 2-1, a).
3. Lower the UniPak™ into position as shown in figure 2-1, b.
4. Press gently on the front edge of the UniPak™ to ensure a good connection (figure 2-1, c).

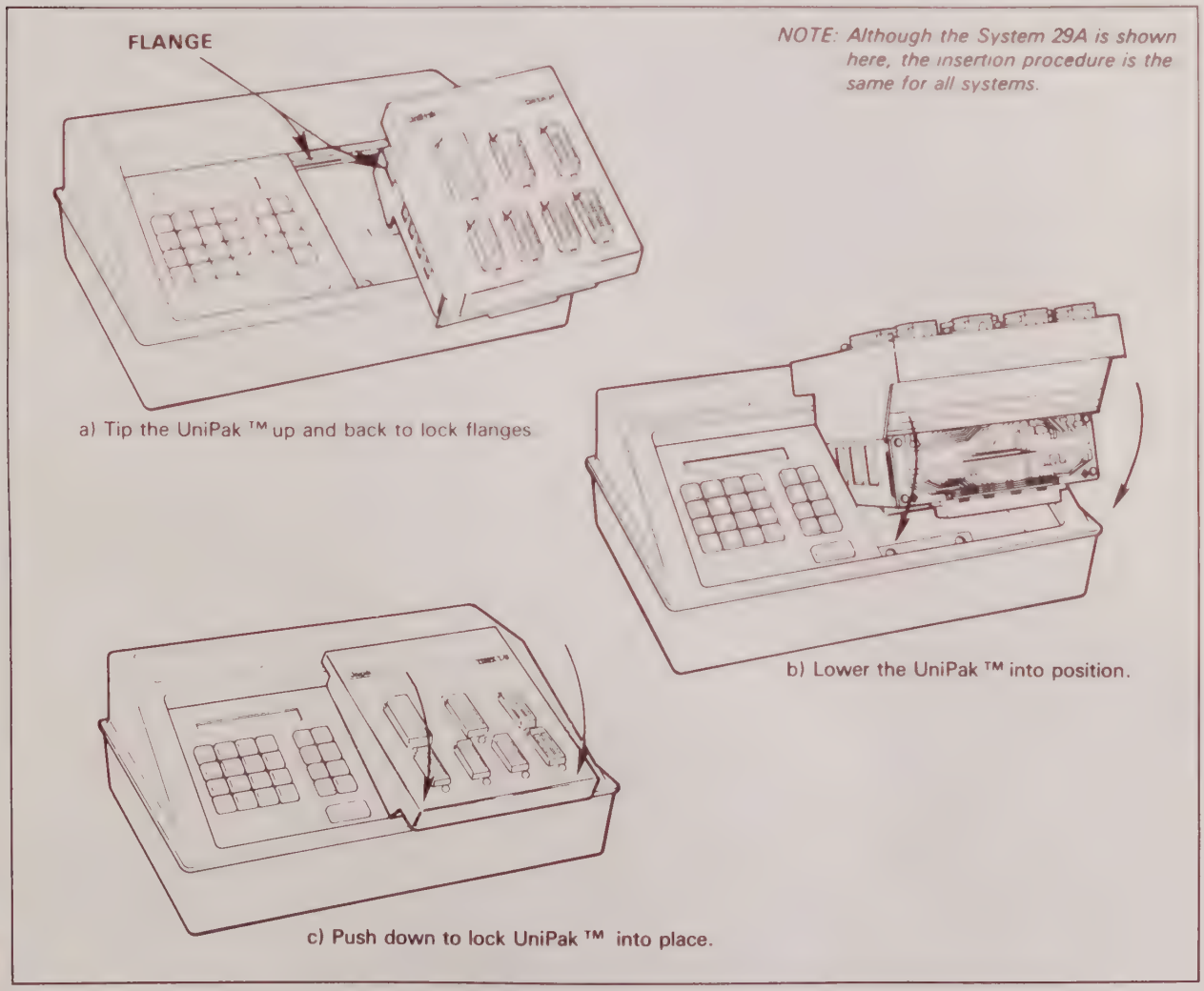


Figure 2-1. UniPak™ Installation

2.3 UniPak™ REMOVAL

1. Check to make sure the programmer is not in the process of an operation. If it is, wait until the operation is complete (the action symbol on the display disappears).
2. Check to make sure a device is not in a socket. If one is in a socket, remove it as described in section 3.7.
3. Tilt the UniPak™ up and gently remove it from the programmer.

2.4 REPACKING FOR SHIPMENT

If the UniPak™ is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by part number, revision level, and name. If the original shipping container is to be used, place the UniPak™ in the container with the appropriate packing material and seal the container with strong tape. If another container is used, be sure that it is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material and seal well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

SECTION 3
OPERATION

3.1 OVERVIEW

The UniPak™ can be used in 29A, 29B, System 19, or 100A programmers of any configuration; see section 1.2 for firmware revision levels required. The typical programming operation with a 29A programmer and a UniPak™ is illustrated in figure 3-1. As can be seen from this figure, the UniPak™ can obtain data from three sources (a master device, a serial port, or the keyboard). Because the serial port and keyboard operations are unique for each type of programmer, you will be referred to your 29A, 29B, System 19, or 100A programmer manual for details on how to program using these mainframes.

When using a master device as the data source to program a blank device, you must first instruct the programmer to copy the device data into programmer RAM (shown as COPY in figure 3-1 and described in section 3.4). Then enter the family code and pinout code as described in section 3.5. The data in the device will have been copied to the RAM of your 29A when you press START, as shown in figure 3-1. You must then remove the master device and instruct the programmer to copy the information just stored in its RAM to a blank device. This completes the basic programming operation.

The procedures to perform basic operations with your UniPak™ are described in this section. You should follow these procedures to properly operate your UniPak™. Wherever possible, key sequences have been included for using your UniPak™ with a 29A Universal Programmer with Rev C firmware (read section 1.2 carefully to determine your programmer's firmware revision level). Refer to your programmer manual for key sequences for the System 19, 29B, and 100A programmers.

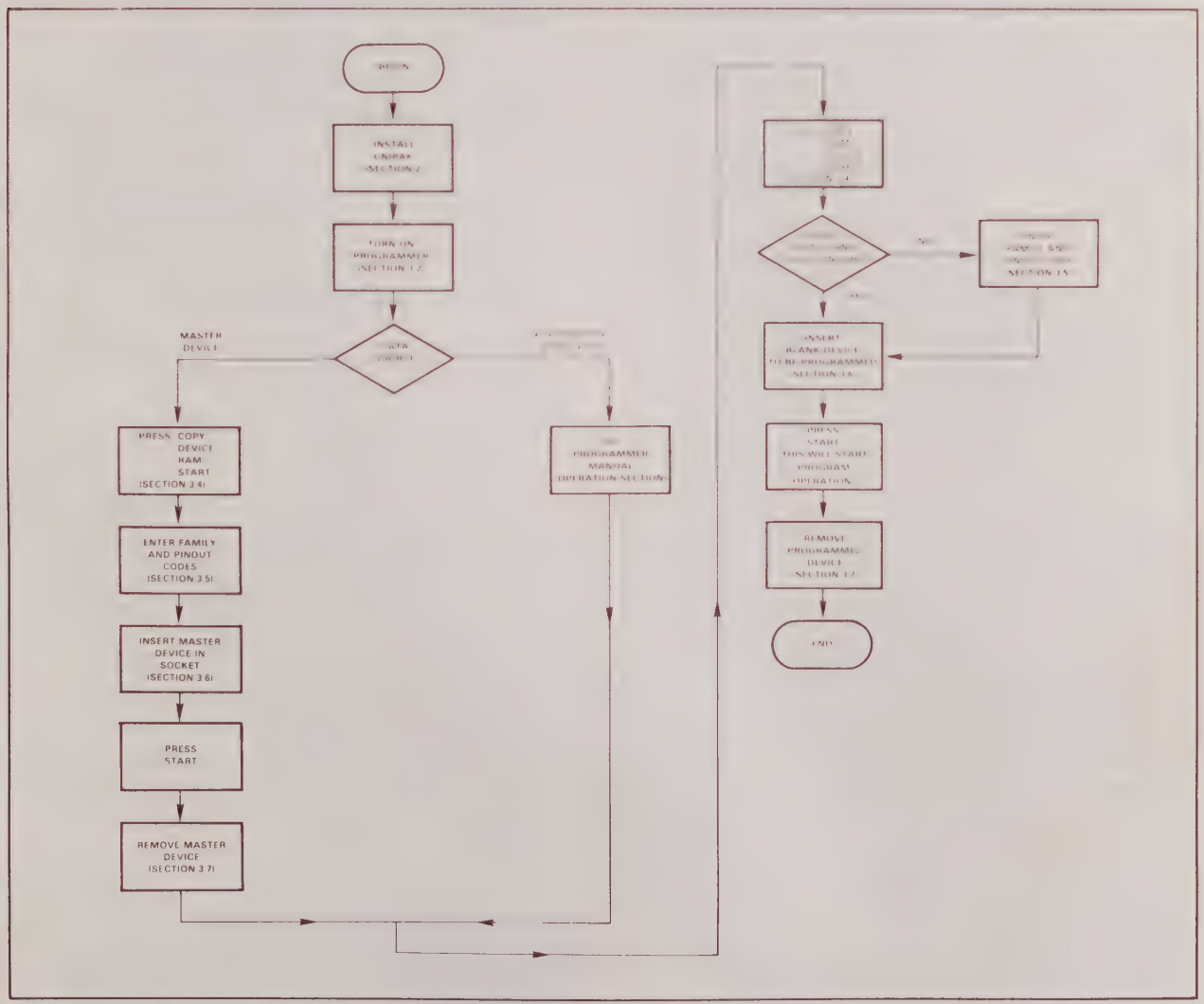


Figure 3-1. Typical 29A Programmer Operation

3.2 POWER UP

NOTE

If the UniPak™ is not installed in the programmer before power is turned on, you will hear a beep until the UniPak™ is installed.

When turned on, the programmer will perform an automatic self-test routine. When the self-test routine is complete, the programmer will signal its readiness.

To turn the programmer on, do the following:

1. Check to make sure a device is not in a socket. If a device is in a socket, lift up the lever (located on the upper left of the socket; see section 3.7), then gently lift the device out of the socket.
2. Plug the AC power cord into the power outlet.
3. Flip the power switch up to the "ON" position (see figure 3-2).

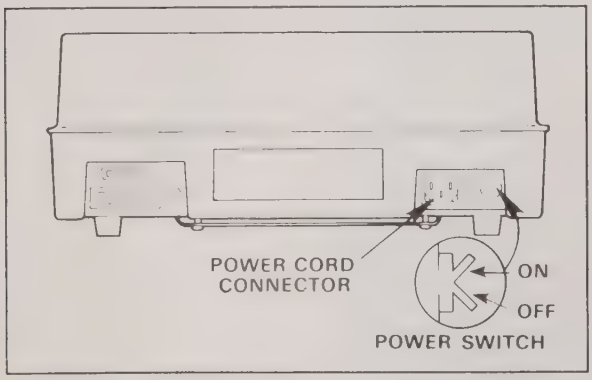


Figure 3-2. Programmer Power Switch Location

3.3 POWER DOWN

CAUTION

Do not turn the power off while the programmer is doing an operation or when a device is in a socket; voltage transients may damage the device.

To turn the programmer power off, do the following procedure:

1. Check to make sure that the programmer is not in the middle of an operation. If it is, wait until that operation is through.
2. Check to make sure a device is not in a socket. If a device is in a socket, remove it as described in section 3.7.
3. Flip the power switch down to the "OFF" position (figure 3-2).

3.4 BASIC OPERATION

All data transfer or verification operations take place between the programmer's internal RAM and the device or between the RAM and serial port in your programmer. Because the procedure to transfer data via a serial port varies from programmer to programmer, this manual describes only data transfer with the 29A. For other programmers, refer to your programmer operation manual.

The basic data transfer operations that can be performed with the UniPak™ and the 29A Universal Programmer are:

- Load RAM with data from a master device (described in section 3.4.1).
- Verify RAM data against the device data (described in section 3.4.2).
- Program a device with RAM data (described in section 3.4.3).

3.4.1 Load RAM With Data From Master Device

To load the 29A RAM with data from a master device, follow the steps listed below.

1. Press COPY; 29A displays COPY DATA FROM
2. Press DEVICE; 29A displays DEV ∧ ADDR/SIZE TO

NOTE

The device is the source of data.

3. Press RAM; 29A displays CO DEV > RAM ∧ ADDR

NOTE

The RAM is the destination of the data from the master device.

4. Press START; 29A displays FAM ∧ ØØ PIN ØØ
5. Enter the family code and pinout code (see section 3.5).
6. Insert the master device into the UniPak™ (see section 3.6).
7. Press START; 29A displays LOADING DEVICE ☐
   LOAD DONE XXXX

NOTE

XXXX is the sumcheck of the device.

8. Remove the master device from the UniPak™ (see section 3.7).

During source destination operations (copy and verify), ADDR and SIZE appear in the 29A prompts. These correspond to starting address and block size, respectively. For more detail on these parameters, see your programmer operation manual. When reading a device, the UniPak™ applies a nominal V_{CC} level. To simulate loading on device outputs, each output is driven by a 1.6 mA current source.

3.4.2 Verify RAM Data Against Master Device Data

The two-pass verify consists of comparing the device data to RAM data and is performed at two V_{CC} levels; these levels, plus the output-sink currents and the output-level-sense voltages, vary according to each manufacturer's requirements.

To verify that data entered in the 29A RAM duplicates the master device data, follow these steps:

1. Press VERIFY; 29A displays VERIFY DATA FROM
2. Press DEVICE; 29A displays DEV ∧ ADDR/SIZE TO

NOTE
The device is the source of data.

3. Press RAM; 29A displays VE DEV > RAM ∧ ADDR

NOTE
The RAM is the destination of the data from the master device.

4. Press START; 29A displays FAM ∧ ØØ PIN ØØ
5. Enter the family code and pinout code (see section 3.5).
6. Insert the master device into the UniPak™ (see section 3.6).
7. Press START; 29A displays VERIFY DEVICE
   VE DEV DONE XXXX

NOTE
XXXX is the sumcheck of the device.

8. Remove the master device from the UniPak™ (see section 3-7).

3.4.3 Program Device With RAM Data

When programming a device, the system performs illegal-bit tests and blank checks at nominal V_{CC} and with nominal output loading.

To program a blank device with the data in the 29A RAM, follow these steps:

1. Press COPY; 29A displays COPY DATA FROM
2. Press RAM; 29A displays RAM ∧ ADDR/SIZE TO
3. Press DEVICE; 29A displays CO RAM > DEV ∧ ADDR
4. Press START; 29A displays FAM ∧ ØØ PIN ØØ
5. Enter the family code and pinout code (see section 3-5).
6. Insert the blank device into the UniPak™ (see section 3-6).
7. Press START; 29A displays TEST DEVICE
   PROGRAM DEVICE
   VERIFY DEVICE
   PRG DONE 01 XXXX
8. Remove the device from the UniPak™ (see section 3.7).

NOTE
XXXX represents the sumcheck of the device.

3.4.4 Extended Select Functions

In addition to the three basic source-destination functions (copy, verify and edit) and the select functions described in the Operation section of your programmer manual, the UniPak™ offers five extended select functions (CC, C3, CE, CF and EF). These functions are not required for normal operation of the UniPak™.

The extended select functions may be used from either the keyboard or from remote control.

Function CC displays the family and pinout codes of the last algorithm moved to RAM, usually the algorithm for the last device programmed or read.

To display the family and pinout codes of the last algorithm moved to RAM, follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press C3 START; 29A displays FXX PYY OPTIONS
3. Press START; 29A displays "NAME OF FIRST OPTION"

To select different options, press the REVIEW key. To execute an option, press START (in terminal remote, the RETURN key is used for the START key, and the space bar is used for the REVIEW key). If the option has subheadings under it, once the START key has been pressed, the REVIEW key can select the desired subheading. The START key is then pressed to execute the subheading. Once an option has been completely executed, an asterisk will be displayed after the option name. Complete execution may require doing a number of subheadings. Pressing the START key a second time after an option is completely executed will exit the options file, and the 29A will display OPTIONS DONE **.

NOTE

For the 8751H, the option "PROG SECTY ONLY" will program the security fuse as soon as the option is selected and executed.

Functions CE and CF are used to set the reject count (the number of programming pulses applied to a fuse or cell before it is rejected); CE sets the reject count back to the commercial specification (this is the default value) and CF sets the single-pulse reject count. This feature was accomplished in older UniPak™ models by adding 50 to the family code.

To select the commercial (default) reject count (CE), follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ^
2. Press CE START; 29A displays SELECT CODE **

To select the single-pulse reject count (CF), take the following steps:

1. Press SELECT; 29A displays SELECT CODE ^
2. Press CF START; 29A displays SELECT CODE **

Function EF calls up a four-digit hexadecimal configuration number and a two-digit decimal version number that correspond to the revision level and version number of the UniPak™ firmware. This function can be useful to identify firmware revision levels when communicating with Data I/O regarding field bulletins and updates.

To display the UniPak™ firmware configuration and version number, do the following:

1. Press SELECT; 29A displays SELECT CODE ^
2. Press EF START; 29A displays XXXX YY **

NOTE

XXXX represents the UniPak™ firmware configuration number, and YY represents the version number.

3.5 FAMILY CODE AND PINOUT CODE SELECTION

Any device that can be programmed with the UniPak™ is specified by a unique combination of a two-digit family code and a two-digit pinout code (table A-1). Once the codes for a particular device are entered, the UniPak™ remains set up for any operation with that device until new codes are entered.

Your programmer manual will tell you where in the key sequence the family and pinout codes should be entered. If you enter invalid family and pinout codes, a beep will sound as you press either START or ENTER, or Err 30 (error 30) will be displayed and the operation will be aborted.

To select the family and pinout codes, procede as follows:

1. Locate the manufacturer name and part number stamped on the device.
2. Go to table A-1, column 1, and find the manufacturer's name.
3. Go to table A-1, column 3, entitled "PROM Part Number" and find the number corresponding to the number on the device.
4. Go to column 4 ("Family Code") and column 5 ("Pinout Code") to find the code numbers corresponding to the device number.
5. Enter the family and pinout codes you selected from table A-1.
6. Push "START."

NOTE

An LED (light-emitting diode) will light under one of the sockets.

Valid family and pinout codes must be in effect to use the System 19 DEVICE DATA key. When you press the DEVICE DATA key, either nominal, first-pass, or second-pass verify levels are applied to the device. The level applied depends on the System 19's position in executing the selected mode. If the KEYBD light is on, the nominal verify level is applied.

3.6 DEVICE INSERTION

Once you have chosen the appropriate family and pinout codes, the UniPak™ is ready to accept a device in the socket located above the lighted LED.

A good electrical connection between the device and the socket is essential. To ensure a good connection, do the following:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift up the lever on the upper left side of the socket above the lighted LED (see figure 3-3). The lever will stay locked in the upright position.
3. Gently insert the device in the socket above the lighted LED. Make sure pin 1 of the device is aligned with pin 1 of the socket, as shown in figure 3-3.
4. Push the lever down to lock the device in the socket.

Once you have entered the family and pinout codes, the UniPak™ is ready for device-related operations. The key sequence to load, program, and verify is described in the Operation section of your programmer manual.

3.7 DEVICE REMOVAL

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Flip up the lever on the left side of the socket (see figure 3-3). The lever will lock in the upright position.
3. Lift the device out of the socket; the LED will remain illuminated.

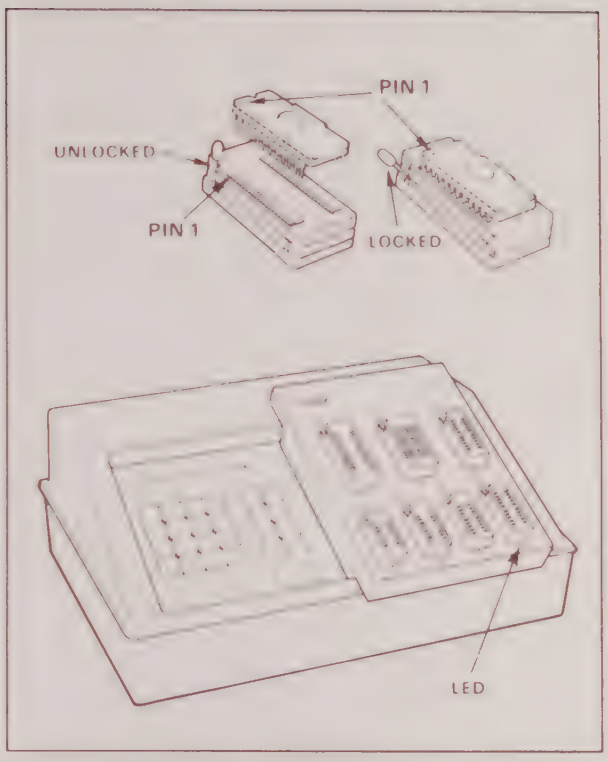


Figure 3-3. UniPak™ Sockets and Device Installation

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SECTION 4
MAINTENANCE/TROUBLESHOOTING/CALIBRATION

4.1 OVERVIEW

The support material in this section has been provided to help you keep your UniPak™ in good operating condition. General maintenance practices are discussed in section 4.2, while the basic troubleshooting steps are listed in section 4.3. For those UniPak™ users who prefer to do their own calibration, detailed procedures, including measurement charts and timing diagrams, are provided in section 4.4.

4.2 MAINTENANCE

Before the UniPak™ can be cleaned (section 4.2.2) and/or inspected (section 4.2.3), it must be disassembled as described below.

4.2.1 UniPak™ Disassembly

To disassemble the UniPak™, refer to figure 4-1 and follow the procedure outlined below.

1. Remove the UniPak™ from the programmer; see section 2.3 for details.
2. Place the UniPak™ face down on a flat surface.
3. Unscrew the captive fasteners (figure 4-1a) until they hang loosely; the screws will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 4-1b) to unlock the flanges.

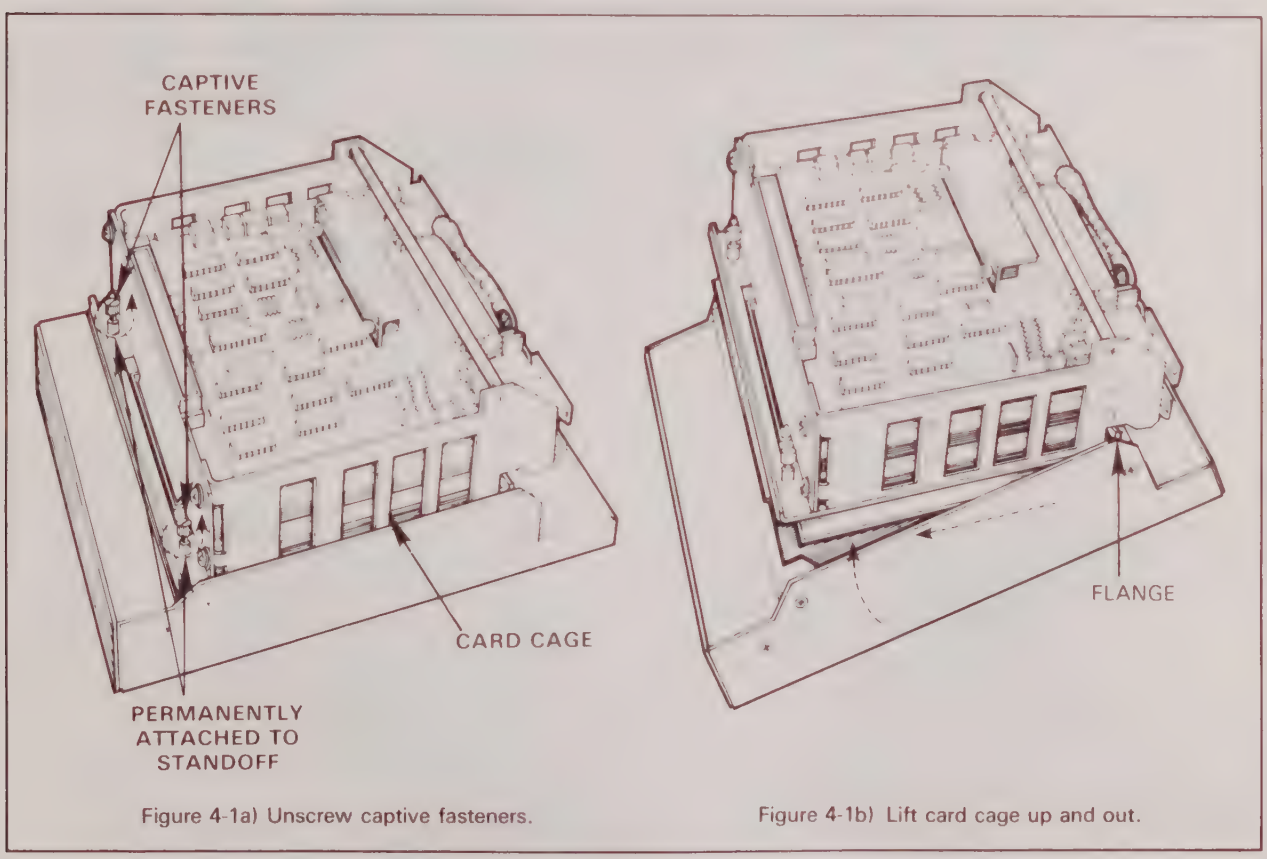


Figure 4-1a) Unscrew captive fasteners.

Figure 4-1b) Lift card cage up and out.

Figure 4-1. UniPak™ Disassembly

5. Lift the card cage up until you can see the socketboard interconnect cable and its connector (figure 4-2).
6. Flip the extraction tabs out on each side of the connector (figure 4-2).
7. Pull the cable out of the connector.
8. Flip the extraction tabs out on the top card (waveform generator card) and unplug the interconnect cable from its connector (figure 4-3).
9. Flip the extraction tabs out on the top card (waveform generator card).
10. Pull the waveform generator card out along the guides (figure 4-3).
11. Repeat steps 9, 10, and 11 for the extraction tabs on the address card.
12. Remove the two screws and the shield, and pull the memory card down to unplug it from the edge connector (as shown in figure 4-4).

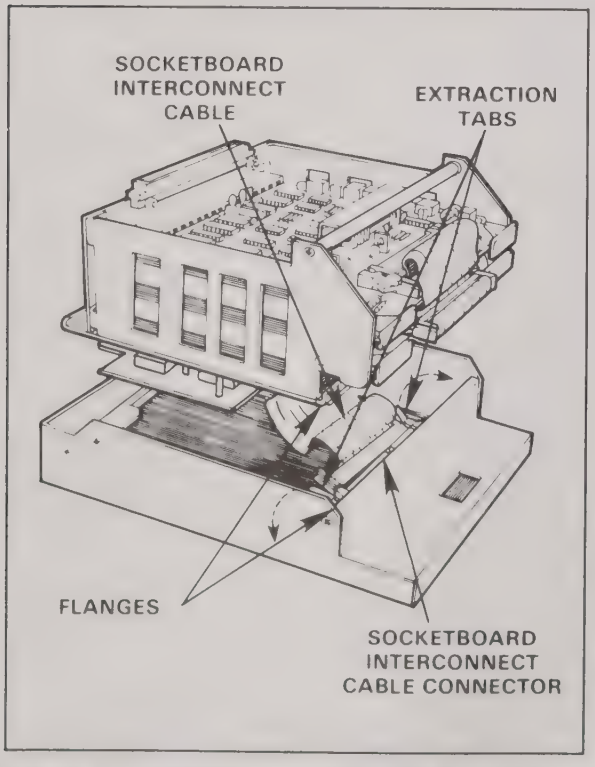


Figure 4-2. Socketboard Interconnect Cable Disconnect

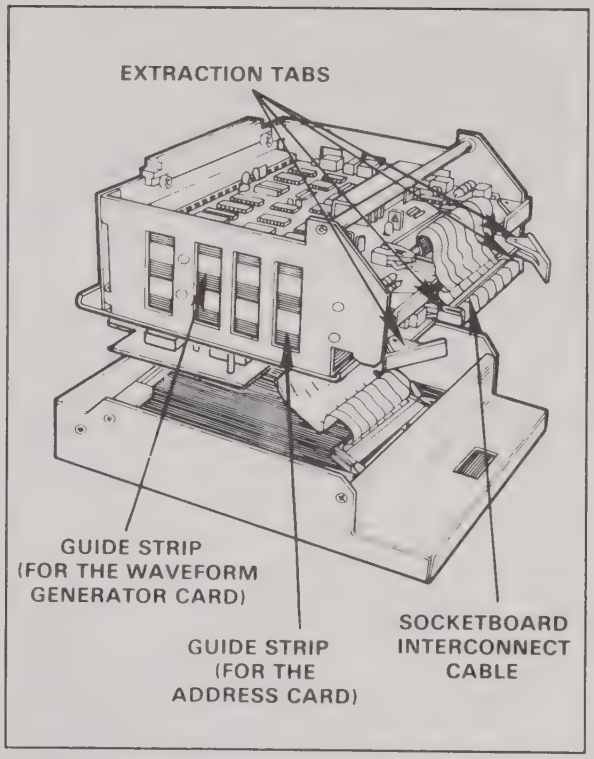


Figure 4-3. Circuit Board Removal

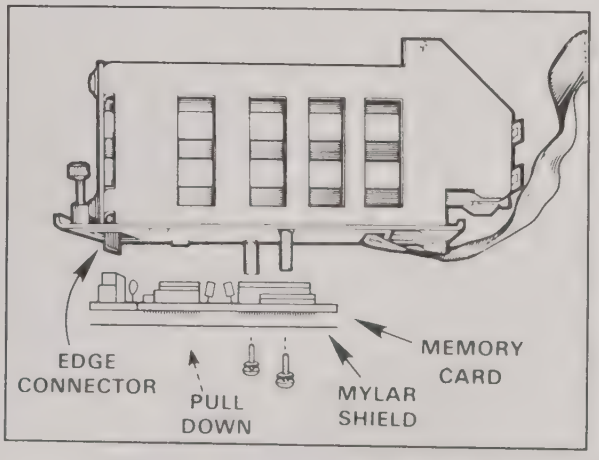


Figure 4-4. Memory Card Removal

4.2.2 Cleaning

Inspect the UniPak™ inside and out for accumulated dirt or dust. To clean the UniPak™, follow the procedure below.

1. Wipe any dust and/or dirt off the outside of the UniPak™ with a clean, damp cloth.

NOTE
Do not use abrasive cleaners or solvents. They will etch the paint.

2. Remove dust from the circuit boards with a blast of dry, compressed air or a clean, soft-bristled brush.

4.2.3 Inspection

You can help prevent malfunctions by periodically inspecting your UniPak™. Check cable connections, card seating, mounting of socketed components, etc., for shorts, opens or unstable continuity.

If you find heat-damaged components, be particularly careful to find and correct the cause of the overheating. This will prevent further damage.

4.2.4 UniPak™ Assembly

1. Plug the memory card onto its edge connector, as shown in figure 4-4.
2. Replace the shield, washers, and the two screws.
3. Flip the two extraction tabs down on the address card.
4. Using the flat surfaces of the extraction tabs, gently push the address card along the guides into its connector.
5. Make sure the extraction tabs on the interconnect cable connector are flipped open.
6. Firmly, but gently, push the socketboard interconnect cable into the connector. Notice that the extraction tabs will move back to their locked positions when the cable is locked into the connector.
7. Repeat steps 3 through 6 to replace the waveform generator card.
8. Plug the socketboard interconnect cable into its connector on the socketboard (figure 4-2).
9. Replace the card cage by tilting it up to lock the flanges, as shown in figure 4-1, then gently setting it down. Make sure the captive fasteners line up with the fastener holes on the UniPak™ frame.
10. Tighten the captive fasteners finger tight.

4.3 TROUBLESHOOTING

This section will help you interpret and isolate failures in the UniPak™. Use it in conjunction with section 5 (Circuit Description) and the schematics provided in the back of this manual.

Three major classes of failures can occur in a system comprised of a programmer and a UniPak™. The first is no system operation, the second is poor yields, and the third is UniPak™ failure.

After successfully troubleshooting the UniPak™, you must calibrate it according to the instructions in section 4.4. It is very important that the programmer be calibrated before the UniPak™ is calibrated.

4.3.1 No System Operation

You should perform the following steps if the system will not initialize with the UniPak™ installed. After completing each step, determine whether the problem still exists.

1. Check to be sure the UniPak™ is properly installed in your programmer.
2. Check the UniPak™ programmer mating connector (J1) for bent or broken pins. (Pin HH is intentionally shorter.)
3. Check the UniPak™ cards to be sure they are correctly installed in their connectors (section 4.2).
4. Check the ribbon cable to be sure it is properly inserted in the connectors (section 4.2).
5. Check the programmer power supplies for proper voltage output levels (see programmer manual).
6. If steps 1 through 5 fail to isolate the problem, contact your local Data I/O Service Center.

4.3.2 Poor Yields

If the yield rate begins to decrease, perform a complete calibration (see Section 4.4). Be sure that the programmer has been calibrated first.

After calibration, if the problem still exists, contact your local Data I/O Service Center.

4.3.3 UniPak™ Failure

Perform the following steps if a device will not program at all or if error messages are displayed. After completing each step, determine whether the problem still exists.

1. Check that the family and pinout codes are correct for the device, and that the device is being inserted in the correct socket.
2. If possible, try a known-good device to determine whether there is a hardware problem.
3. Check to be sure the UniPak™ is properly installed.
4. Check the UniPak™ programmer mating (J1) connector for bent or broken pins. (Pin HH is intentionally shorter.)
5. Check the UniPak™ cards to be sure they are correctly installed in their connectors (section 4.2).
6. Check to be sure the ribbon cable is correctly oriented and properly inserted in the connectors.
7. Perform a complete calibration, noting any measurements falling outside the indicated limits. Refer to the corresponding test number in table 4-1 for suspected boards and components, as well as the circuit description (section 5) and the schematics, to attempt to isolate the problem.
8. Perform waveform observations and note any discrepancies. Referring to the circuit description and the schematics may be helpful in isolating the problem.
9. If steps 1 through 8 fail to resolve the problem, contact your local Data I/O Service Center.

Table 4-1. Troubleshooting Chart

TEST NUMBER	SUSPECT BOARDS	SUSPECT COMPONENTS
1	701-1998	U26, U13, CR1
2	701-1998	Q1, Q2, U14
3	701-1998	U19, U13, Q3
4	701-7997	VR1, Q23, U6, U13
5	701-7997	Q17, U8, U4, U11
	702-7995	U2, CR12
6	701-7997	Q8, U1, U4, U10, Q2, Q7, Q14, Q24, Q1
7	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
8	701-1998	U26, U13, CR1
9	701-1998	U26, U13, Q3
10	701-1998	U26
11	701-7997	U13, U14, U7, Q13, Q1, Q9
	701-1998	U18, Q4-11, U16, U17
12	701-7997	U12, U11, U4, U8, Q17
	702-7995	CR12, U2
13	701-7997	U12, U9, U4, U3, Q10
14	701-7997	U12, U10, U4, U1, Q8
15	701-1998	U25, U26, U13, CR1
16	701-1998	U25, U19, U13, CR1, Q3
17	701-7997, 701-1998	
18	702-7995	DS2, U1
19	701-7997	U1, CR8, U6, Q16, R39
20	701-7997	Q8, U1, U4, U10, Q2, Q7, Q14, Q24, Q1
21	701-7997	Q1, Q4, Q2, Q20
22	701-7997	Q1, Q18, Q21
23	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
24	701-7997	Q6, Q12, CR7, Q22
25	701-7997	U11, U4, U8, Q17
26	701-7997	U10, U4, U1, Q8
27	701-7997	Q15, U4, Q21
28	701-7997	VR2, U7
29	701-7997	U11, U4, U8, Q17
30	701-7997	U12, U10, U4, U1, Q8, CR1, CR2, U5, U2, U7, Q1, Q2, U6, Q18, CR11, Q19, Q21, Q15, Q5, U11
31	701-7997	U11, U4, U8, Q17
32-35	701-1998	RP1, RP2, U3-6
	702-7995	U9, U10, Q2
36	702-7995	DS1, U1
37	702-7995	U1, CR8
38	701-1998	U1, U2, U12, Q12-19
39	701-1998	U1, U2, U12, Q12-19
40	701-1998	U1, U2, U12, Q12-19
41	701-1998	U1, U2, U12, Q12-19
42	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
43	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
44	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
45	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
46	702-7995	DS3, U1
47	702-7995	U2, CR14
48	702-7995	DS4, U1
49	702-7995	U2, CR15
50	702-7995	DS5, U1
51	702-7995	U2, CR11
52	702-7995	DS6, U1
53	702-7995	U2, CR13
54	702-7995	DS7, U1
55	702-7995	U2, CR16
56	702-7995	Q1, RP1, U3, CR17

4.4 CALIBRATION

The need for calibration varies with the amount of use your UniPak™ receives. Generally, we suggest calibration whenever: 1) programming yields fall below the manufacturer's recommended minimums, or 2) troubleshooting has been completed, or 3) the user's company policy requires periodic calibration certification.

NOTE

If calibration or repair is required but you lack the facilities to accomplish it, contact the nearest Data I/O Service Center.

Because of differences in programmer mainframes, this manual does not attempt to cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the UniPak™.

Calibration of the UniPak™ consists of three parts:

1. Power Supply Calibration—measures the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this part of the calibration procedure must be done first. Refer to your programmer manual.
2. DC Calibration—consists of measuring and adjusting critical DC voltage levels generated by the UniPak™.
3. Waveform Observation—enables observation of waveforms on an oscilloscope to ensure compliance with the device manufacturers' critical voltage and timing specifications.

The first part of the calibration procedure (power supply calibration) varies with the type of programmer you have. Therefore, this manual refers you to your programmer manual for details on power supply calibration.

DC calibration is discussed in section 4.4.1.

The following equipment is necessary to calibrate the UniPak™:

- Data I/O calibration extender (part number 910-1521)
- Three and a half-digit digital voltmeter (DVM)
- Dual-trace oscilloscope (Tektronix 465 or equivalent)

Check the appropriate programmer manual for any additional equipment that you may need to calibrate the programmer.

To prepare your UniPak™ for calibration, follow the procedures outlined below:

1. Turn the programmer power off; see section 3.3 for details.
2. Remove the UniPak™ from the programmer; see section 2.3 for details.
3. Insert the calibration extender into the programmer the same way you insert the UniPak™ (section 2.2).
4. Unscrew the two thumb screws (captive fasteners) located on the underside of the top cover of the UniPak™ (figure 4-1); they connect the card cage to the socket assembly. Separate the two parts of the assembly.

CAUTION

Do not let the fasteners short to the motherboard.

5. Insert the 64-pin connector of the card cage into the mating connector on the calibration extender (figure 4-5, detail B).
6. Lean the top portion of the UniPak™ against its bottom portion at a 45-degree angle (see figure 4-5).

NOTE

Be sure the socket assembly flange locks into the card cage flange (see figure 4-5, detail A).

Do not allow the frame of the socket assembly to short to the memory board.

Be careful not to strain the cable or scratch the top of the programmer.

4.4.1 DC Calibration

The DC calibration procedure described in this section enables you to adjust critical DC voltage levels generated by the UniPak™. To follow this procedure, use the measurement chart at the end of this section. This measurement chart contains the information needed for all DC calibration tests. This information is included on the measurement chart in columns with the following headings:

- Step No.—tells which step to use for each test. Step numbers are set at the programmer keyboard and reflected in the display.
- Test No.—identifies individual tests.
- Test Description—identifies the functions being tested.
- Measurement Test Location—tells which socket pins, circuit boards, or test points to probe for measuring voltages.
- Measurement—specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the UniPak™ until the problem is corrected.
- Adjustment Location—tells which potentiometer to adjust if a measurement is out of range.
- Comments—gives special instructions for particular tests.

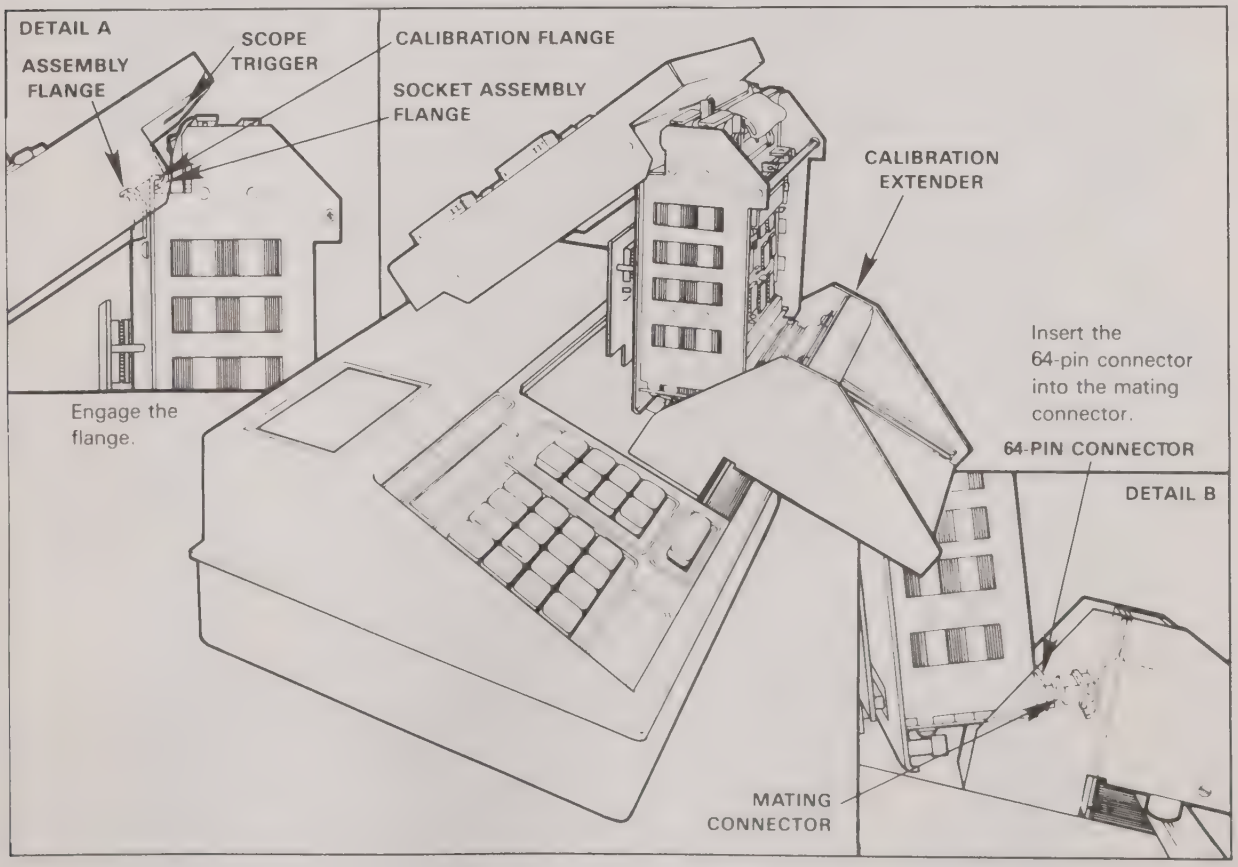


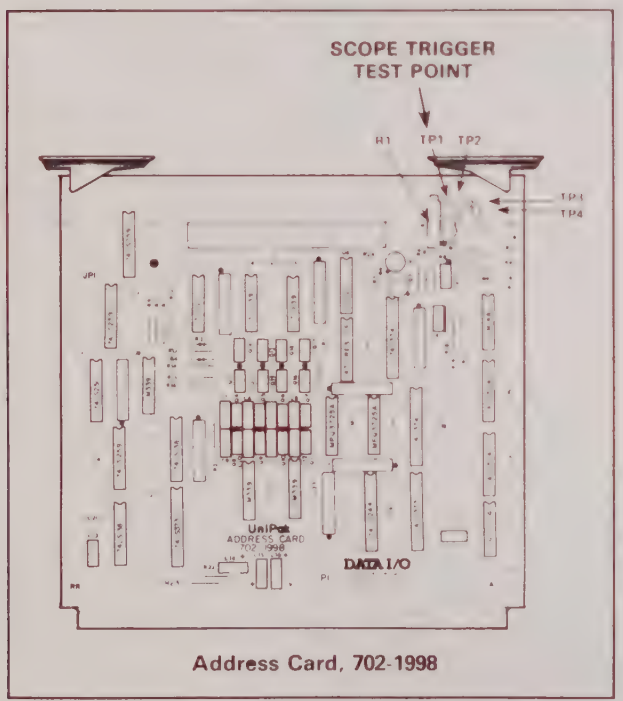
Figure 4-5. Calibration Setup

The DC calibration procedure is as follows:

CAUTION

Remove all devices from the sockets before entering the calibration mode (see section 3.8 for details). Waveform generation may damage any device in the UniPak™ sockets.

1. Turn the programmer power on (section 3.2).
2. Put the programmer into the calibration mode by following the key sequences in table 4-2.
3. Perform the general calibration steps (steps 1 through 20) on the measurement chart. For steps 4 and 5, refer to the figures at the end of the measurement chart to observe the bit switch rise waveform and the DAC step waveforms. Trigger your oscilloscope by connecting to the test point under the top edge of the socket assembly (see figure 4-6).



Address Card, 702-1998

Figure 4-6. UniPak™ Scope Trigger Test Point

Table 4-2. Key Sequence To Access the Calibration Mode

Programmer System	Key Sequence To Enter Calibration Mode	To Increment Step No.	To Decrement Step No.
19	Press SELECT Press C2 Press ENTER Enter Step Number* Press START	Press ENTER	Press REVIEW
29A 29B	Press SELECT Press C1 Press START Enter Step Number* Press START	Press START	Press REVIEW
100A	Press SELECT Press 12 Enter Step Number* Press START	Press START	Press BACK SPACE

*Optional

For each general calibration step on the measurement chart do the following:

- Take measurement readings at the device sockets or test points indicated on the measurement chart; figure 4-7 shows the pin numbers for the sockets; figure 4-8 shows test points.
- Ground the digital voltmeter to socket 7, pin 10 on the front panel of UniPak™.

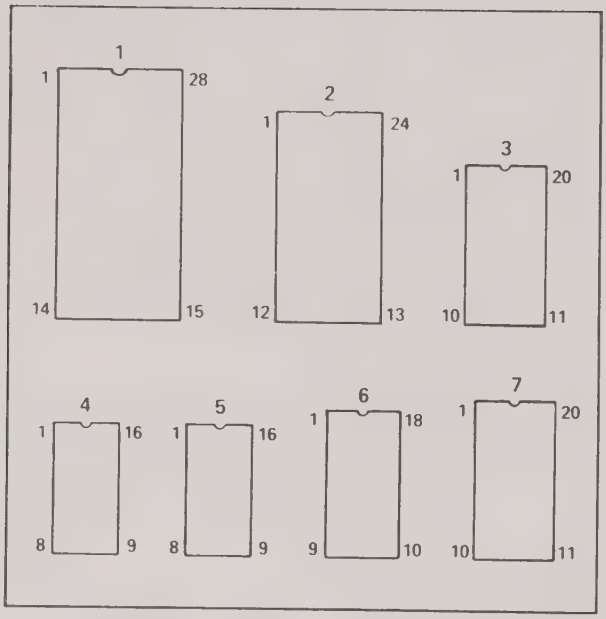
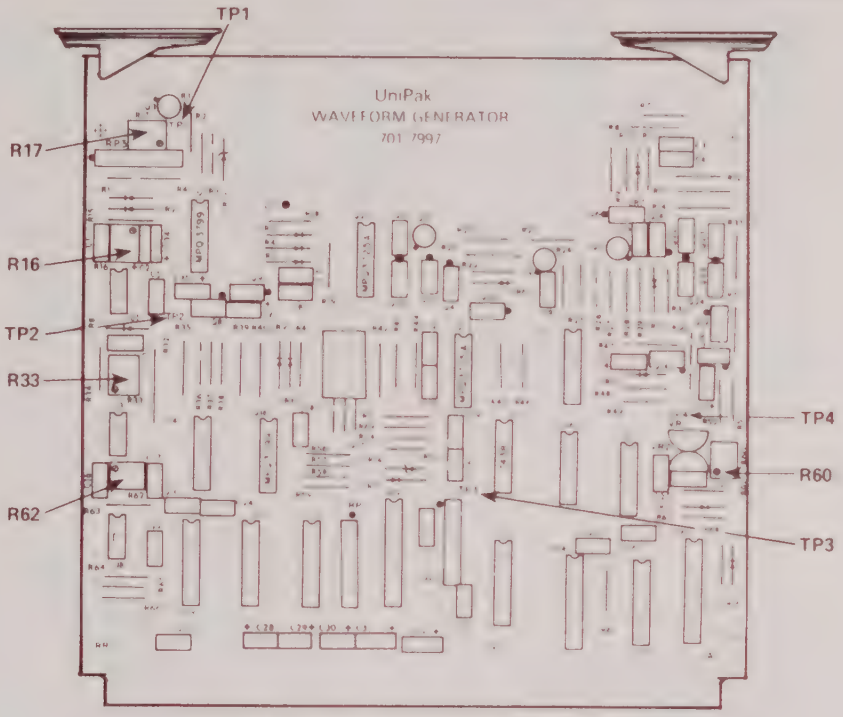
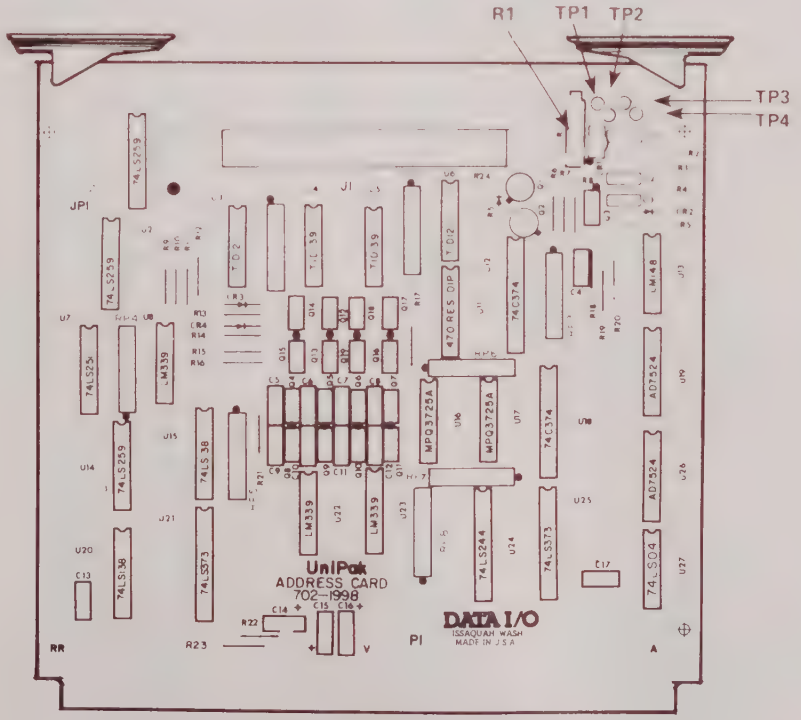


Figure 4-7. Pin Numbers of Device Sockets

- The adjustment pots on the waveform generator, memory board, and the address card enable you to make adjustments when your measurements do not match the measurement chart; figure 4-7 shows the location of these adjustment points.
- Access each new step by pressing the START (or ENTER) key. The new step number will appear in the display when the UniPak™ is ready for the next step. To go back to a previous test, press the REVIEW (or BACKSPACE) key.



a. Waveform Generator, 701-7997



b. Address Card, 702-1998

Figure 4-8. Adjustment Locations

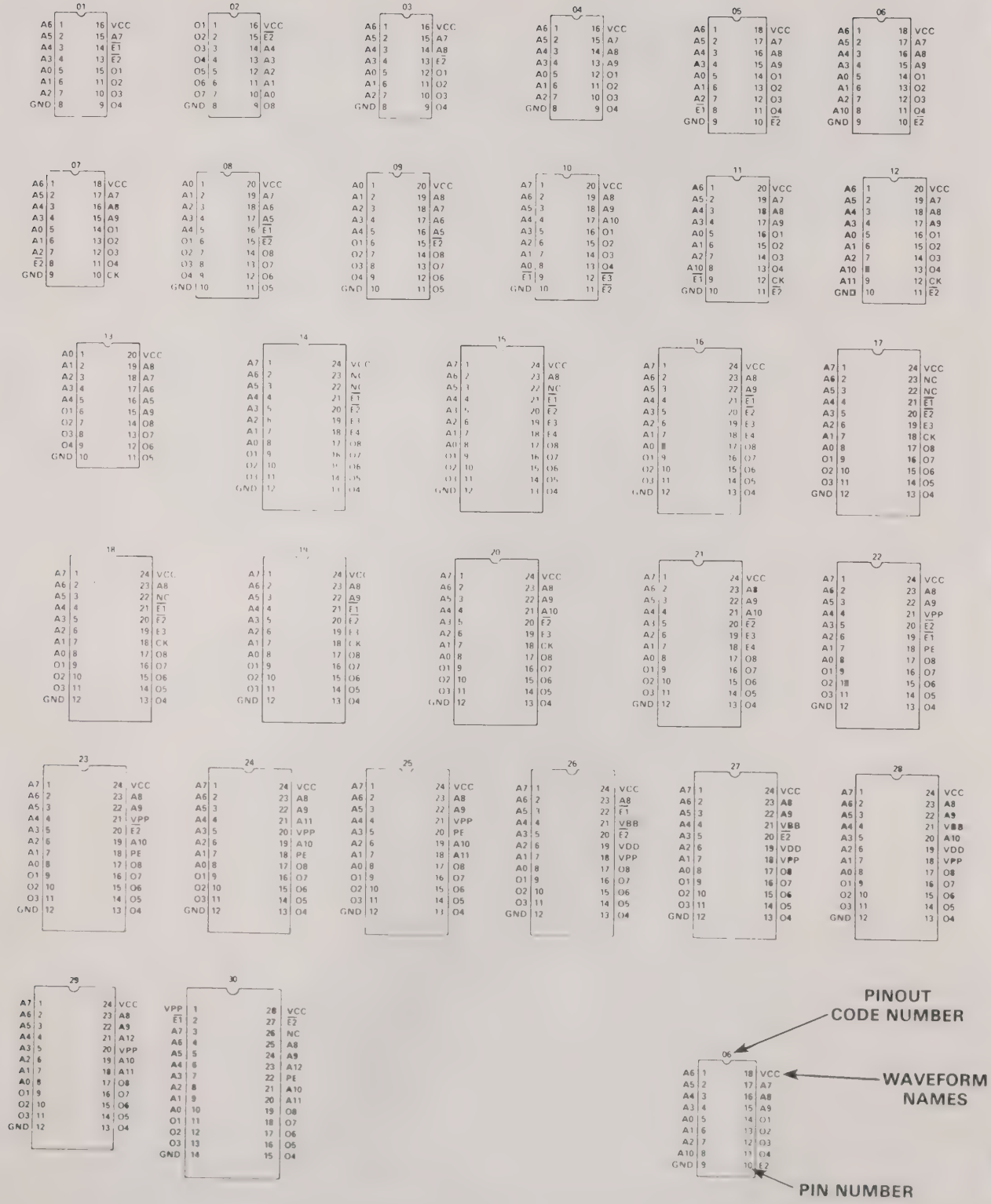


Figure 4-9. Pin Names by Pinout Code Numbers

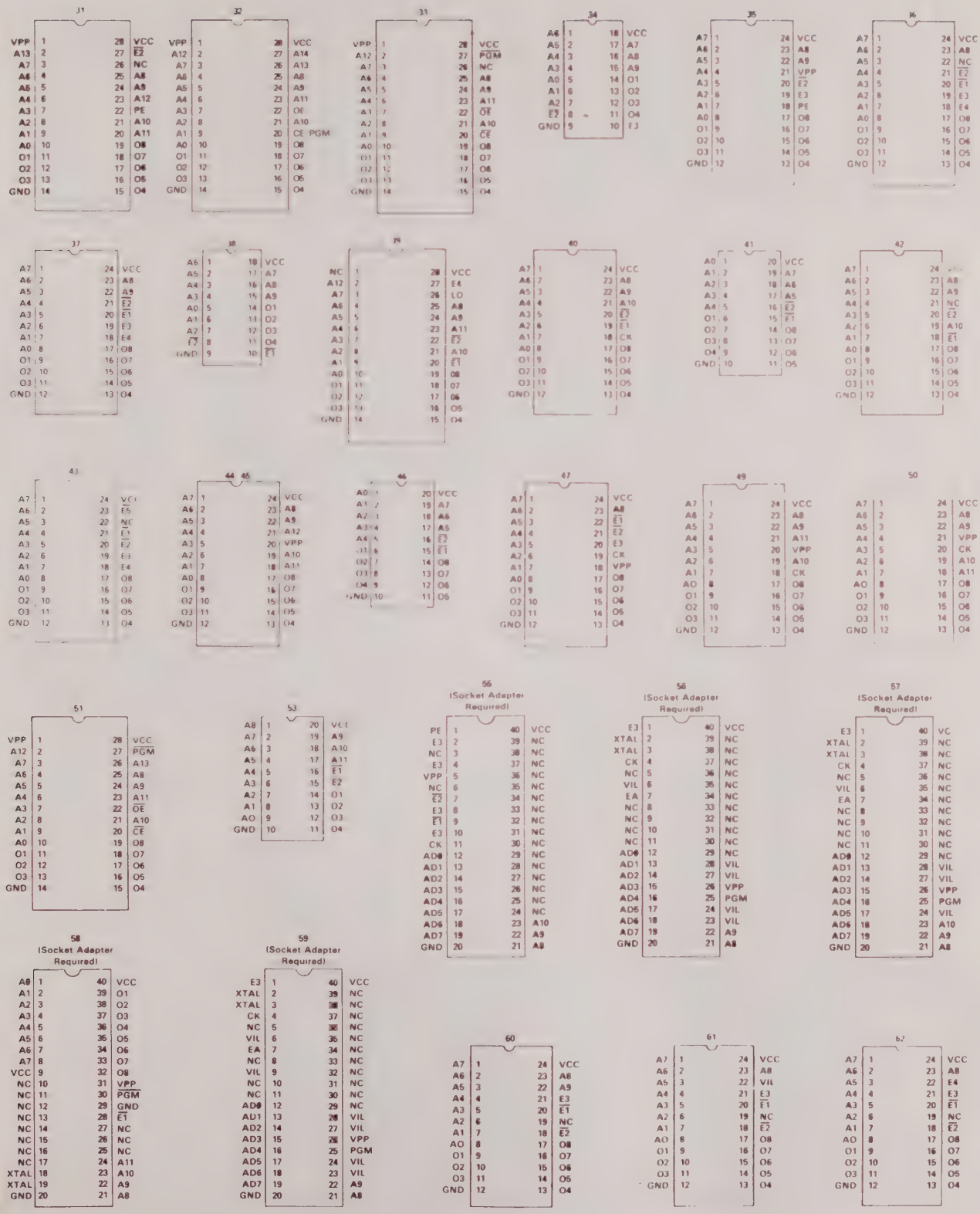


Figure 4-9. Pin Names by Pinout Code Numbers (Continued)

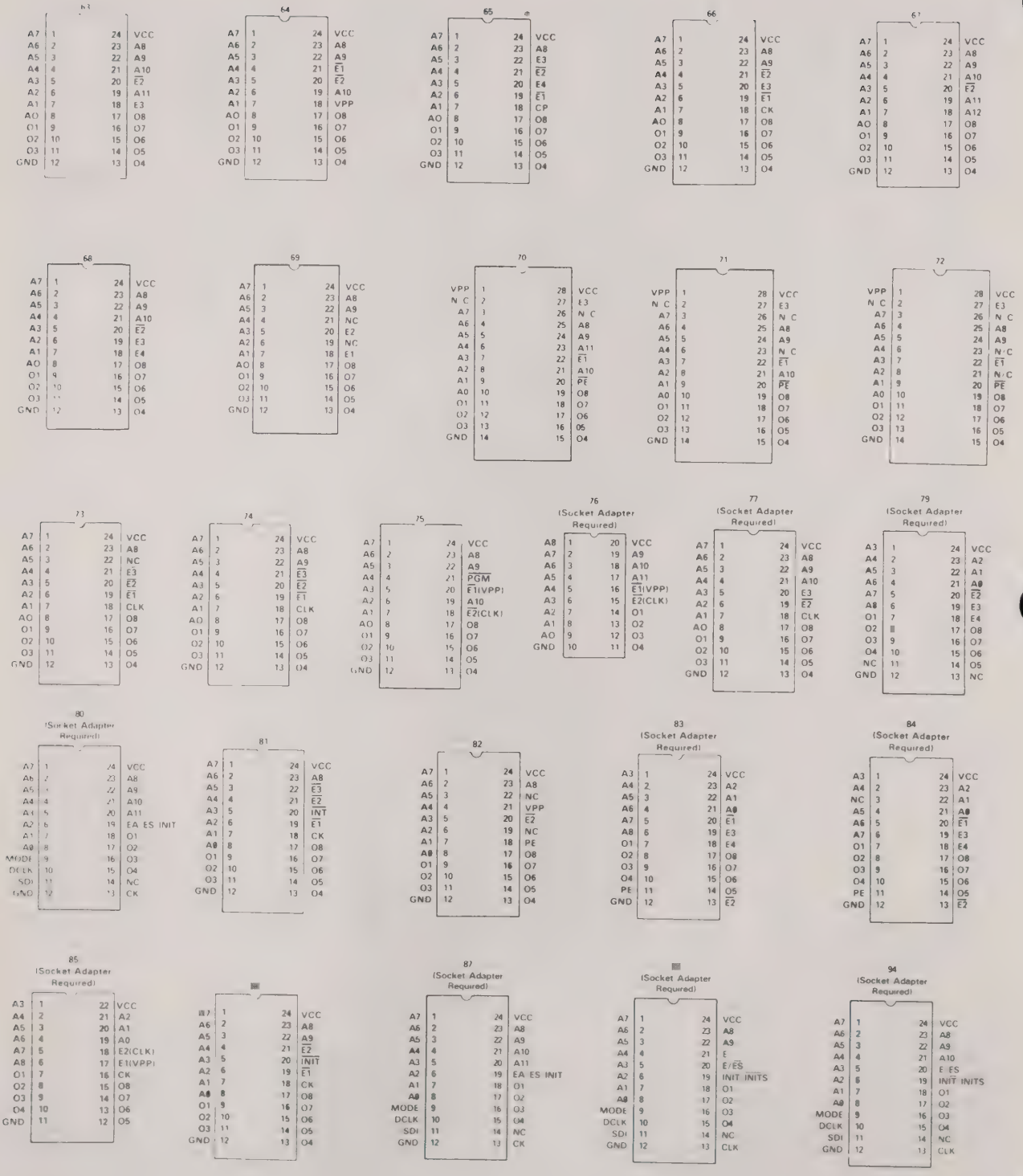


Figure 4-9. Pin Names by Pinout Code Numbers (Continued)

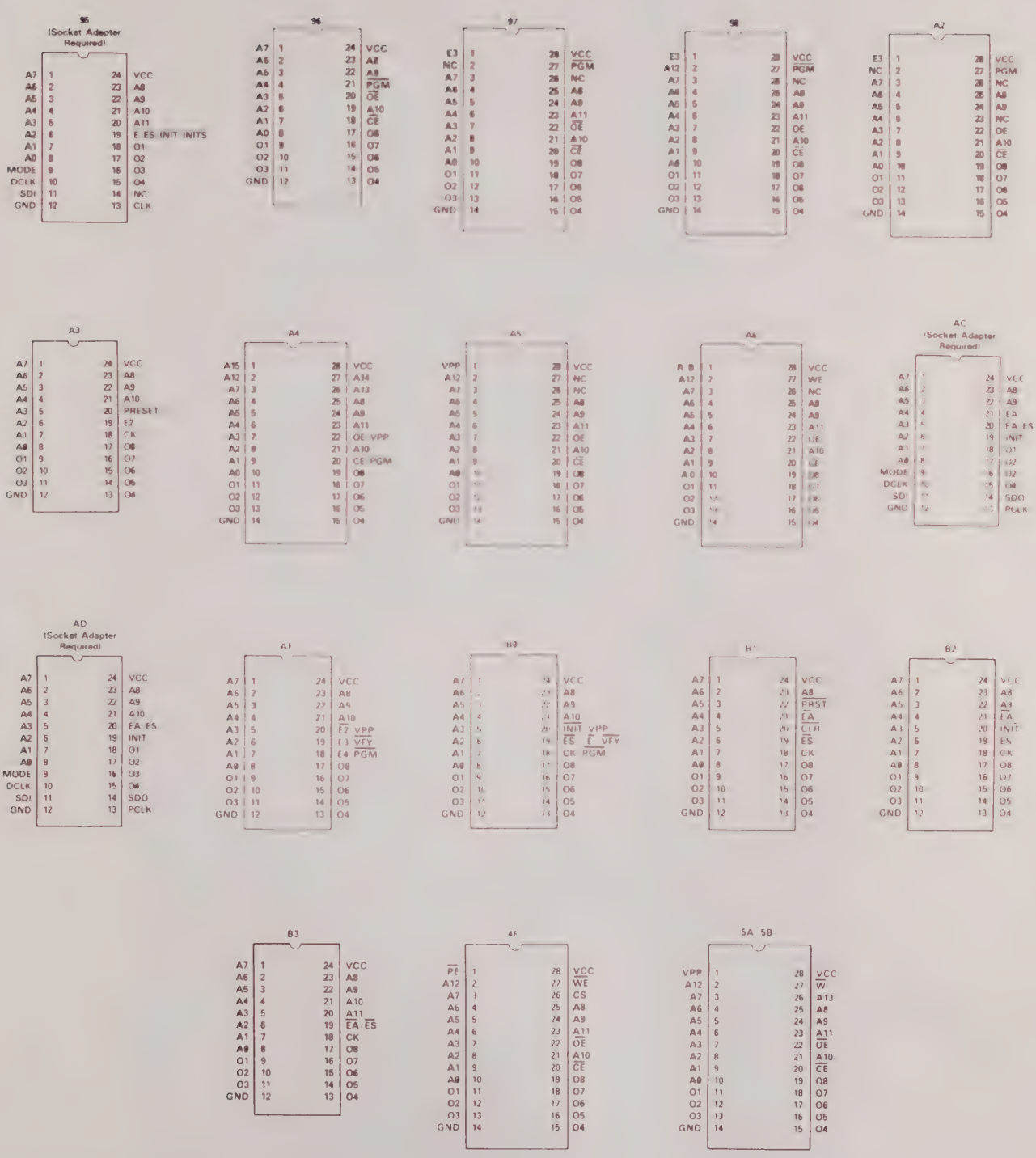


Figure 4-9. Pin Names by Pinout Code Numbers (Continued)

Table 4-3. Measurement Chart

REVISIONS

LTR	DESCRIPTION	P E	DATE
	[illegible]		2/84

UniPak™ Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
			The following tests are performed					
			with the UniPak™ on the calibration					
			extender:					
			Socket/Pin					
1	1	V reference supply	701-1998/TP4	10.20V	10.24V	10.28V	R1,701-1998	
	2	Load supply (high range)	701-1998/TP2	24.3V		25.7V		
	3	Load supply (low range)	701-1998/TP3	24.3V		25.7V		
	4	Supply reference	701-7997/TP4	4.98V	5.00V	5.02V	R60, 701-7997	
	5	V_{CC} supply	2 24	11.9V	12.0V	12.1V	R62,701-7997	
	6	Ct supply	2 20	32.7V	33.0V	33.2V	R16,701-7997	
	7	Bit supply	2 9	25.7V	26.0V	26.2V	R33,701-7997	
2	8	V reference supply	701-1998/TP4	6.70V		6.90V		
	9	Load supply	701-1998/TP3	10.3V		11.7V		
3	10	V reference supply	701-1998/TP4	3.30V		3.50V		

Table 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P E	DATE
D	ECN 5022		2/84

UniPak™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pin	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
4	11	Bit switch rise waveform	2 14				R17, 701-7997	See waveform photograph (page 4-27)
5		DAC step waveforms						
	12	V_{CC}	2 24					See waveform photograph (page 4-28)
	13	Bit supply	701-7997/TP2					See waveform photograph (page 4-29)
	14	CE supply	701-7997/TP1					See waveform photograph (page 4-28)
	15	V_{REF} supply	701-1998 TP4					See waveform photograph (page 4-29)
	16	Load supply	701-1998/TP3					See waveform photograph (page 4-26)
			The following tests are performed					
			with the UniPak™ installed in its					
			normal operating position.					
6	17	All voltages off	all all	-11.5		.4		
7	18	Socket 2 LED						Confirm that socket 2 LED is on
	19	V_{CC} supply load	2 24	11.5		12.5		Place a 20-ohm, 2W resistor between pins 24 and 12, socket 2

Table 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P E	DATE
D	ECN 5022		2784

UniPak^{tm} Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pin	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
8	20	CE supply load	2 20	32.3V		33.2V		Place a 100-ohm, 10W resistor
								between pins 20 and 12,socket 2.
	21	Pin 18 voltage switch	2 18	32.7V		33.2V		
	22	Pin 21 voltage switch	2 21	32.7V		33.2V		
9	23	Bit supply load	2 11	25.2V		26.0V		Place a 100-ohm, 5W resistor
								between pins 11 and 12,socket 2.
	24	Pin 19 voltage switch	2 19	24.9V		25.5V		
10	25	V_{CC} voltage linearity	2 24	3.90V		4.10V		
	26	CE supply linearity	2 18	23.0V		23.5V		Place a 2.2K-ohm, 1/2W resistor
								between pins 12 and 18,
								socket 2.
	27	-5V supply	2 21	-5.2V		-4.8V		
	28	12V supply	2 20	11.4V		12.6V		
11	29	V_{CC} voltage linearity	2 24	4.90V		5.10V		

Table 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P E	DATE
D	ECN 5022		2/84

UniPak™ Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pin	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
	30	CE supply linearity	2 21	11.4V		12.6V		
12	31	V_{CC} voltage linearity	2 24	4.9V		5.1V		
	32	I source and pulldowns	2 9,11,14,16	2.0V		2.4V		
	33	I source and pulldowns	2 10,13,15,17	2.0V		2.4V		
13	34	I source and pulldowns	2 10,13,14,17	2.0V		2.4V		
	35	I source and pulldowns	2 9, 11, 14 16	2.0V		2.4V		
14	36	Socket 1 LED						Confirm that socket 1 LED is on.
	37	V_{CC} voltage supply	1 28	4.9V		5.1V		
	38	Odd address and data	1 2,3,5,7,9,11,13,15,17,	2.0V		2.4V		
		high	20,22,24,26					
	39	Even address and data	1 1,4,6,8,10,12,15,17,19,21,	-0.1V		0.4V		
		low	23,25,27					
15	40	Odd address and data	1 2,3,5,7,9,11,13,16,18,	-0.1V		0.4V		
		low	20,22,24,26					
	41	Even address and data	1 1,4,6,8,10,12,15,17,19,21,	2.0V		2.4V		
		high	23,25,27					
16	42	Odd data lines high	1 11,13,16,18	24.5V		25.5V		
	43	Even data lines pullups	1 12,15,17,19	4.9V		5.1V		

Table 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P E	DATE
D	EC# 5022		2/24

UniPak^{tm} Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pin	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
17	44	Odd data lines pullups	1 11,13,16,18	4.5V		5.5V		
	45	Even data lines high	1 12,15,17,19	25.5V		26.5V		
18	46	Socket 3 LED						Confirm that socket 3 LED is on.
	47	V_{cc} voltage supply	3 20	4.90V		5.10V		
19	48	Socket 4 LED						Confirm that socket 4 LED is on.
	49	V_{cc} voltage supply	4 16	4.90V		5.10V		
20	50	Socket 5 LED						Confirm that socket 5 LED is on.
	51	V_{cc} voltage supply	5 16	4.90V		5.10V		
21	52	Socket 6 LED						Confirm that socket 6 LED is on.
	53	V_{cc} voltage supply	6 18	4.90V		5.10V		
22	54	Socket 7 LED						Confirm that socket 7 LED is on.
	55	V_{cc} voltage supply	7 20	4.90V		5.10V		
23	56	V_{cc} pullup 1 on	1 28	4.0V		5.2V		
		V_{cc} pullup 2 on	2 24	4.0V		5.2V		
		V_{cc} pullup 3 on	3 20	4.0V		5.2V		
		V_{cc} pullup 4 on	4 16	4.0V		5.2V		
		V_{cc} pullup 5 on	5 16	4.0V		5.2V		
		V_{cc} pullup 6 on	6 18	4.0V		5.2V		
		V_{cc} pullup 7 on	7 20	4.0V		5.2V		

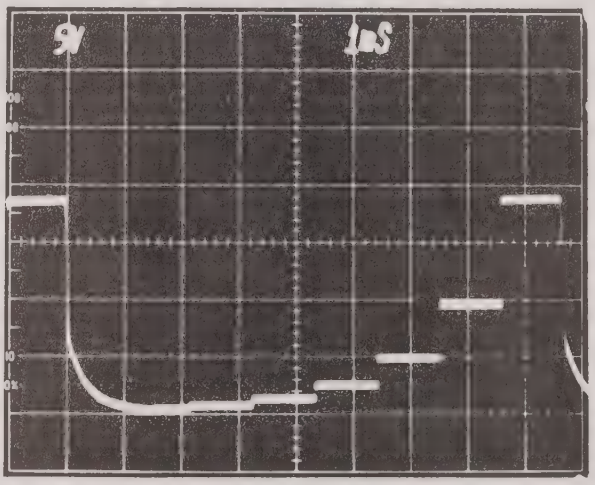
Sheet 5 of 5

Measurement Chart

Measurement Chart

PROGRAM ELECTRONICS _____

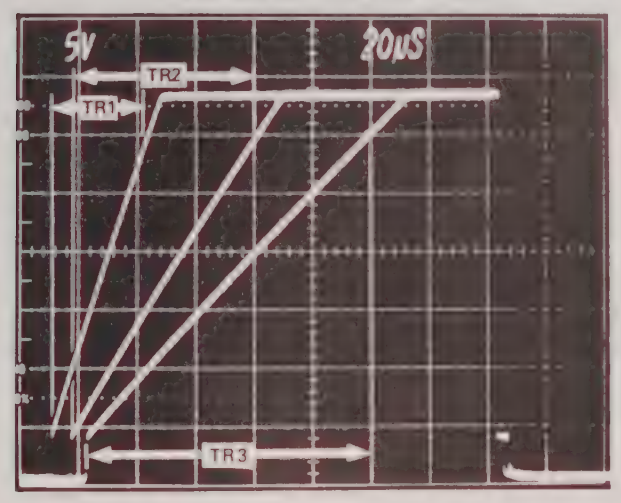
DAC Step Waveform



DAC Load Supply

DATE	REV	REVISION RECORD	DR	CK
3 84				

Bit Switch Rise-Time Waveform



	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	TR1	26	33	37	µs	
	TR2	62	66	70	µs	Adjust R17, 701-7997
	TR3	90	100	110	µs	

NOTE: All TR's are measured from 10% to 90%

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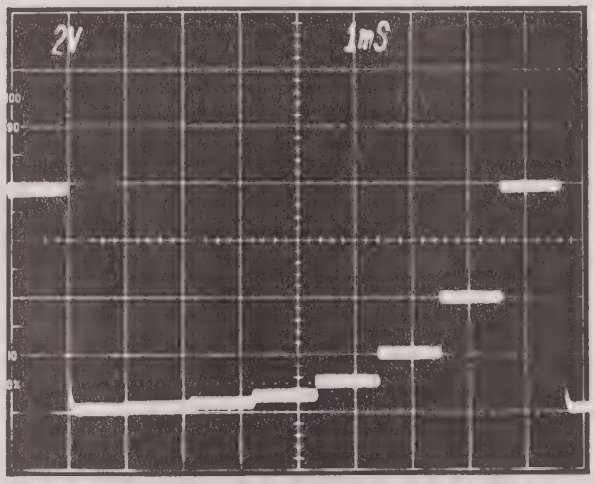
Measurement Chart

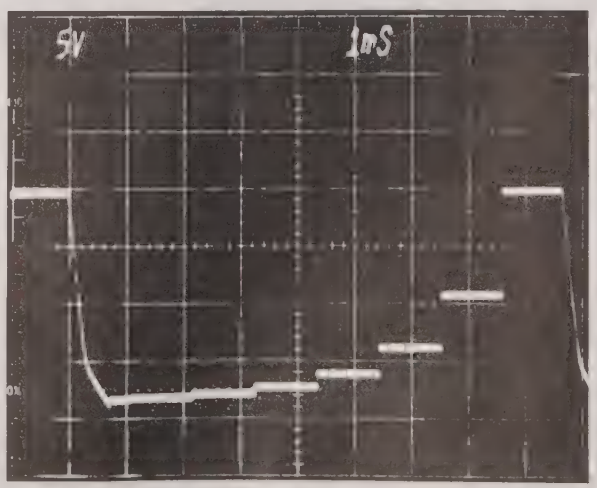
PROGRAM ELECTRONICS _____

DAC Step Waveform



V_{CC} DAC

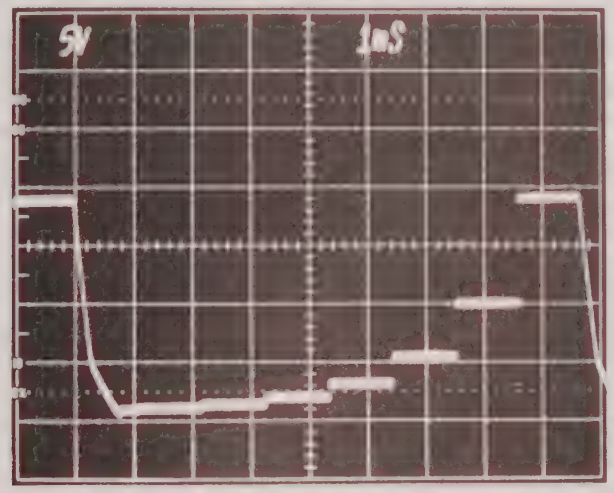
DAC Step Waveform



$\overline{CE}$ Supply DAC

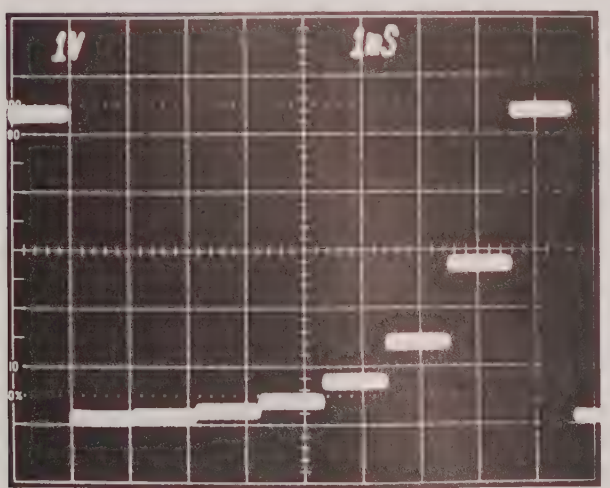
DATE	REV	REVISION RECORD	DR	CK
3 84				

DAC Step Waveform



Bit Supply DAC

DAC Step Waveform



V_{REF} Supply DAC

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SECTION 5
CIRCUIT DESCRIPTION

5.1 OVERVIEW

This section defines the functions of UniPak™ principal hardware components. Each circuit-card assembly is depicted by a block diagram accompanied by a written description.

5.2 GENERAL ARCHITECTURE

5.2.1 The Link Between the UniPak™ and the Programmer

The UniPak™ is controlled by the programmer's extended processor bus (J6), through the UniPak™'s mating connector. Pin functions of the extended processor bus are shown in table 5-1.

The control software for the UniPak™ is located in EPROM on the memory card (702-0045).

5.2.2 The Buses

The programmer's address bus, data bus, R/$\overline{W}$ line and $\overline{V \bullet \emptyset_2}$ line access the software on the memory card and control the gates and registers on the waveform generator (701-7997) and address and data driver cards (701-1998). The UniPak™'s device bus gathers the programming waveforms produced by these cards and transmits them to the socket card (702-7995). Figure 5-1 shows the relationships between the buses.

Table 5-1. Pin Functions, Programmer's Extended Processor Bus (at J1-J3)

Pin	Function	Pin	Function
1	A_0	A	A_8
2	A_1	B	A_9
3	A_2	C	A_{10}
4	A_3	D	A_{11}
5	A_4	E	A_{12}
6	A_5	F	A_{13}
7	A_6	H	A_{14}
8	A_7	J	A_{15}
9	DO_0	K	DI_0
10	DO_1	L	DI_1
11	DO_2	M	DI_2
12	DO_3	N	DI_3
13	DO_4	P	DI_4
14	DO_5	R	DI_5
15	DO_6	S	DI_6
16	DO_7	T	DI_7
17	Ver A	U	Ver B
18	Start	V	Clk inh
19	W L	W	26
20	VOL VOH	X	36
21	+ 5V	Y	9V
22	+ Proq	Z	+ 24V
23	GND	AA	5V
24	Sense	BB	Operate
25	+ 48 V	CC	Unreg. H.V
26	GND	DD	Gnd
27	C1	EE	C4
28	C2	FF	C5
29	C3	HH	C6
30	IRQ	JJ	Gate Enable
31	R W	KK	Extend
32	V•Ø2	LL	+ 18V Raw
33	Interlock	MM	PP
34	+ 10V Raw	NN	RR
35	Write	PP	Read
36	Reset	RR	Fwd

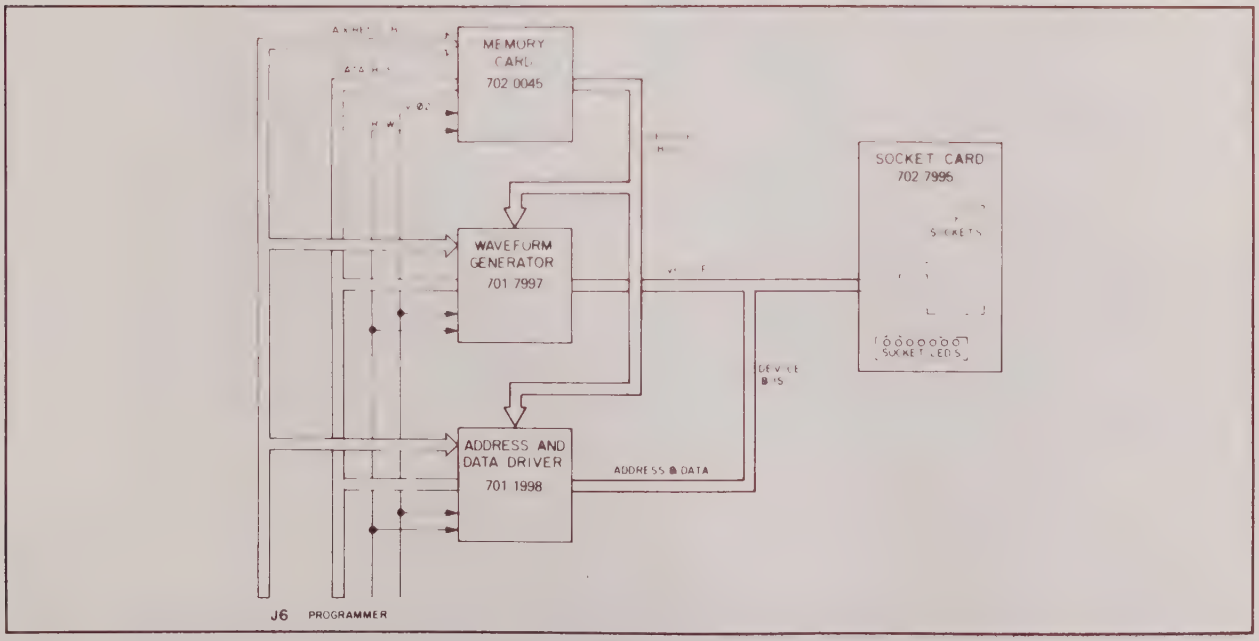

Figure 5-1. Block Diagram, UniPak™ Electronics

5.3 COMPONENT LAYOUT

Figure 5-2 shows the component layout of the UniPak™. The principal components are described in paragraphs 5.3.1 through 5.3.5.

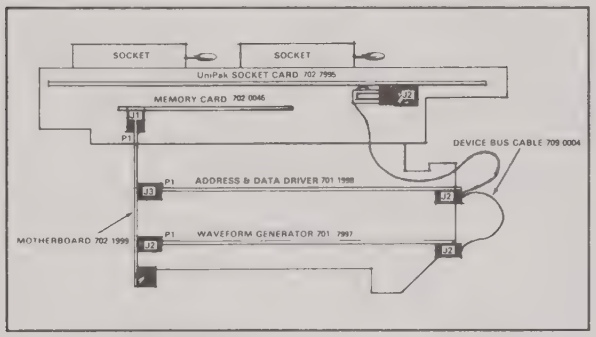

Figure 5-2. Principal Components of the UniPak™

5.3.1 Motherboard

The motherboard accepts the signals and power supplies from the J6 of the programmer and transmits them to two identical 72-pin edge connectors and a 50-pin edge connector (see figure 5-3 and schematic 008-1999).

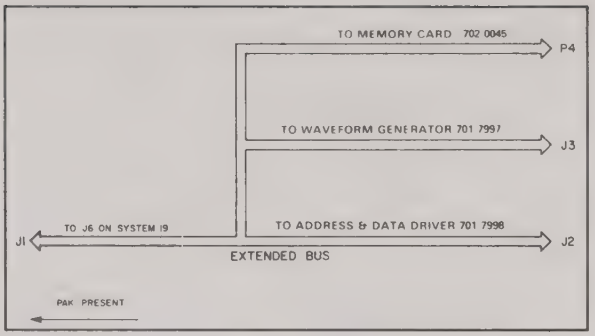

Figure 5-3. Block Diagram, UniPak™Motherboard

5.3.2 Waveform Generator

The waveform generator provides all signals, including addresses and data, required for programming devices. These signals are generated by the blocks shown in figure 5-4.

Three major supplies are the V_{CC} supply, the CE supply and the bit supply, which are used to generate the respective signals. Each supply is software-controlled via a D/A converter. All DACs obtain their reference voltage from the DAC reference.

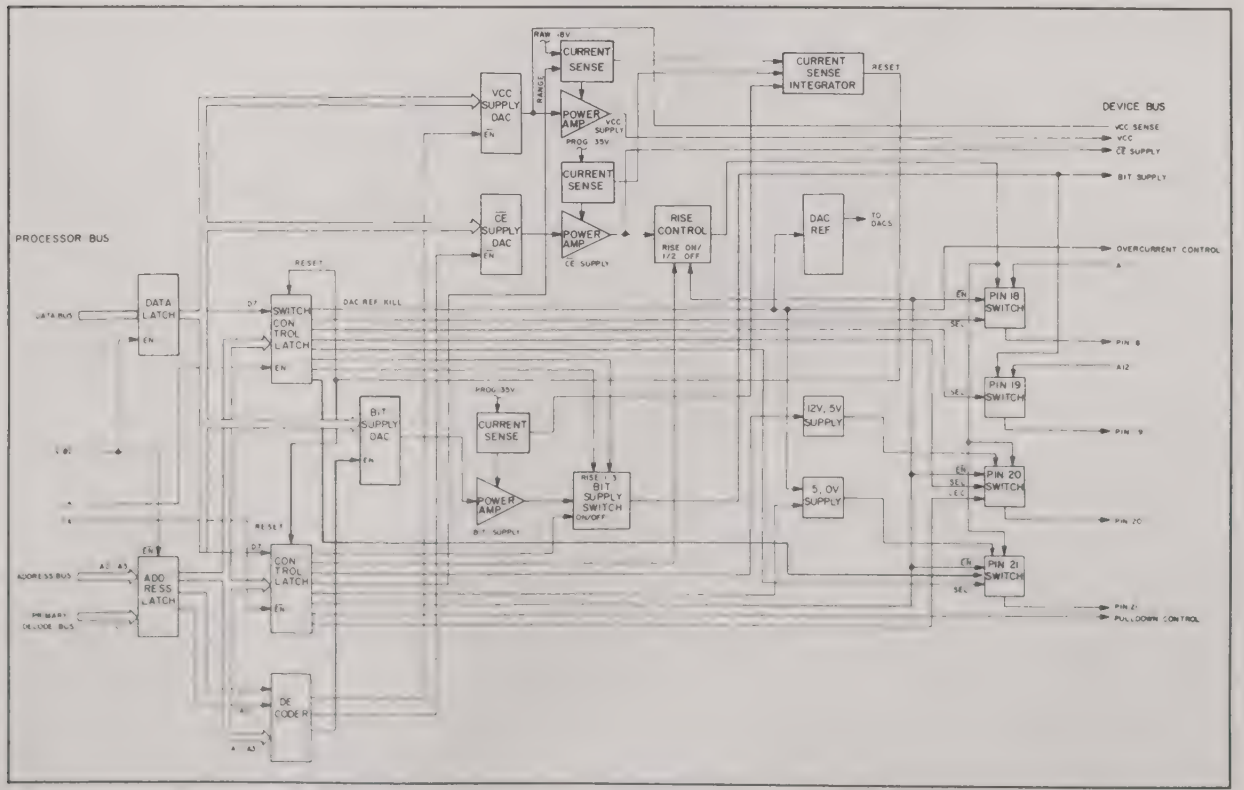

Figure 5-4. Block Diagram, Waveform Generator

The V_{CC} waveforms are generated by writing appropriate DAC values from the firmware. The rise and fall times are fixed by the slewing rate of the op amp. Two overcurrent detectors are included, one for low currents and one for high currents (above 1 amp). If a detector is activated, the control latch is reset; the DAC-reference kill output then causes the DAC reference to go to zero, in turn causing all supplies to return to zero.

The V_{CC} supply senses the V_{CC} voltage at the PROM socket via the V_{CC}-sense line. This remote sensing compensates for all cable drops between the supply and the socket.

The $\overline{CE}$ waveforms are generated by using the $\overline{CE}$ supply in conjunction with one of the pin switches. The voltage level is selected by writing the appropriate value to the $\overline{CE}$ DAC. One of two rise times is selected by the control latch and rise-time control circuitry. Either the pin 18, 20 or 21 switch can be enabled by the switch-control latch to output the high-level $\overline{CS}$ voltage. Switches that are not enabled can output TTL levels.

Each pin switch consists of an emitter follower with the collector tied to the $\overline{CE}$ supply. A current source is provided for the base of each switch to charge the common rise-time capacitor. When the base is released, a linear ramp is generated which is truncated at the $\overline{CE}$-supply level. An NPN-transistor pulldown is included in the switch to provide a 20V/μs-controlled fall time. Logic circuitry prevents the pulldown and pullup circuits from being active simultaneously.

The pin 21 switch uses the same principles as the pin 18 and pin 20 switches. However, a power amplifier output (-5V/0 supply) provides the ground reference for the switch. For certain programming algorithms this amplifier output is brought to -5V.

The pin 20 switch includes a pullup that is connected to the +12/+5V supply, thus allowing the switch in the TTL mode to switch from 0 to 12V as well as from 0 to 5V. The +12/+5V supply consists of a monolithic regulator and a 5.1V zener diode controlled by the switch-control latch.

Signals to be applied to the data lines of a device are generated with the bit-supply signals and controlled by the bit-supply switch. The bit supply is nearly identical to the $\overline{CE}$ supply, but has one less diode in the feedback path, compensating for one less drop in the switch paths. The bit-supply switch consists of an emitter follower, a current source, and three rise-time control capacitors. The collector of the emitter follower is connected to the bit supply; the base is connected to the current source and timing capacitor. The control latch can select the timing capacitor and also control the base of the switch. When the base is released, the output ramps linearly to the bit-supply level. The output on the bit-supply switch is sent to the address and data driver card and to the pin 19 switch. Unlike the pin 18, 20 and 21 switches, the pin 19 switch consists of a simple PNP-saturating switch controlled by the switch-control latch.

The current-sense integrator smoothes the transient overcurrent pulses occurring from charging supply capacitors. When an overcurrent condition from the V_{CC}, $\overline{CE}$, bit or 0/-5V supply exists for sufficient time, the control latch is reset, in turn causing the DAC reference and the supplies to go to zero. The state of the overcurrent-control line can be read by the address and data driver card and used by the programmer to detect shorted devices. Table 5-2 lists the functions of the device-bus pins. The data latch buffers the data bus and holds data to satisfy the long DAC data-hold requirement. The address latch buffers the lower-order address lines and the primary decode bus. These buffered lines are then sent to the decoder and the address latches. The decoder provides decode signals to the DACs for the V_{CC}, $\overline{CE}$ and bit supplies. The switch-control latch and the control latch receive their clocks from a decoder on the address and data driver card.

Table 5-2. Pin Functions, Device Bus (at J1)

1	PA_8	26	PA_7
2	PA_9	27	PA_6
3	PA_{10}	28	PA_5
4	PA_{11}	29	PA_4
5	PA_{12}	30	PA_3
6	PA_{13}	31	PA_2
7	PA_{14}	32	PA_1
8	PA_{15}	33	PA_0
9	GND	34	VCC
10	VCC Sense	35	GND
11	CE Supply	36	GND
12	Bit Switch	37	Bit Supply
13	Pin 20	38	Pin 18
14	Pin 21	39	Pin 19
15	Scope Trigger	40	PD_1
16	-9	41	PD_2
17	+24	42	PD_3
18	Overcurrent	43	PD_4
19	Pull Down Control	44	S1
20	VCC Pullup	45	S2
21	VREF	46	S3
22	PD_8	47	Spare
23	PD_7	48	Spare
24	PD_6	49	+5
25	PD_5	50	GND

5.3.3 Address and Data Driver

The address and data driver, diagrammed in figure 5-5, provides the device address, device data, data loads and supply measurement capability of the UniPak™.

The address drivers consist of addressable latches driving the device address bus. The addressable latches receive data from the most-significant-bit line of the data bus.

The data switch register drives PNP data switches which direct the output of the bit switch to the appropriate device-data line. The PNP switches are driven by current sources to provide a constant-base drive at all bit-switch voltages.

The data sink register drives the NPN data sinks directly. These data sinks are used to shunt to ground large programming currents. Device data is read via the data comparators and strobed to the processor bus via the data gate. The comparators receive their reference voltage from the V_{REF} amplifier, which is controlled by the V_{REF} DAC. Loading the device data bus is controlled by the load DAC, the load amplifier and the high/low-range load switch. A voltage is developed by the load amp and applied to either the high-range or low-range resistor banks. The diode clamps limit the voltage applied by the load resistors to the data bus to approximately 5V.

The supply comparators read the V_{CC}-sense line, the $\overline{CE}$ supply and the bit-switch line. The comparator gate/multiplexer strobes the data from the supply comparators and the overcurrent-read line to the most-significant-bit line of the data bus.

The socket-select latch provides a control line for the high-/low-range switch and control lines for the socket card.

The data latch buffers the data bus and holds data to satisfy the DAC requirements.

The address latch buffers low-order addresses for the secondary decoder. The decoder provides the appropriate signals for the DACs and registers as well as the latches on this card and on the waveform generator. The $\overline{V \bullet \emptyset_2}$ signal controls the timing of the various clock signals developed by the decoder.

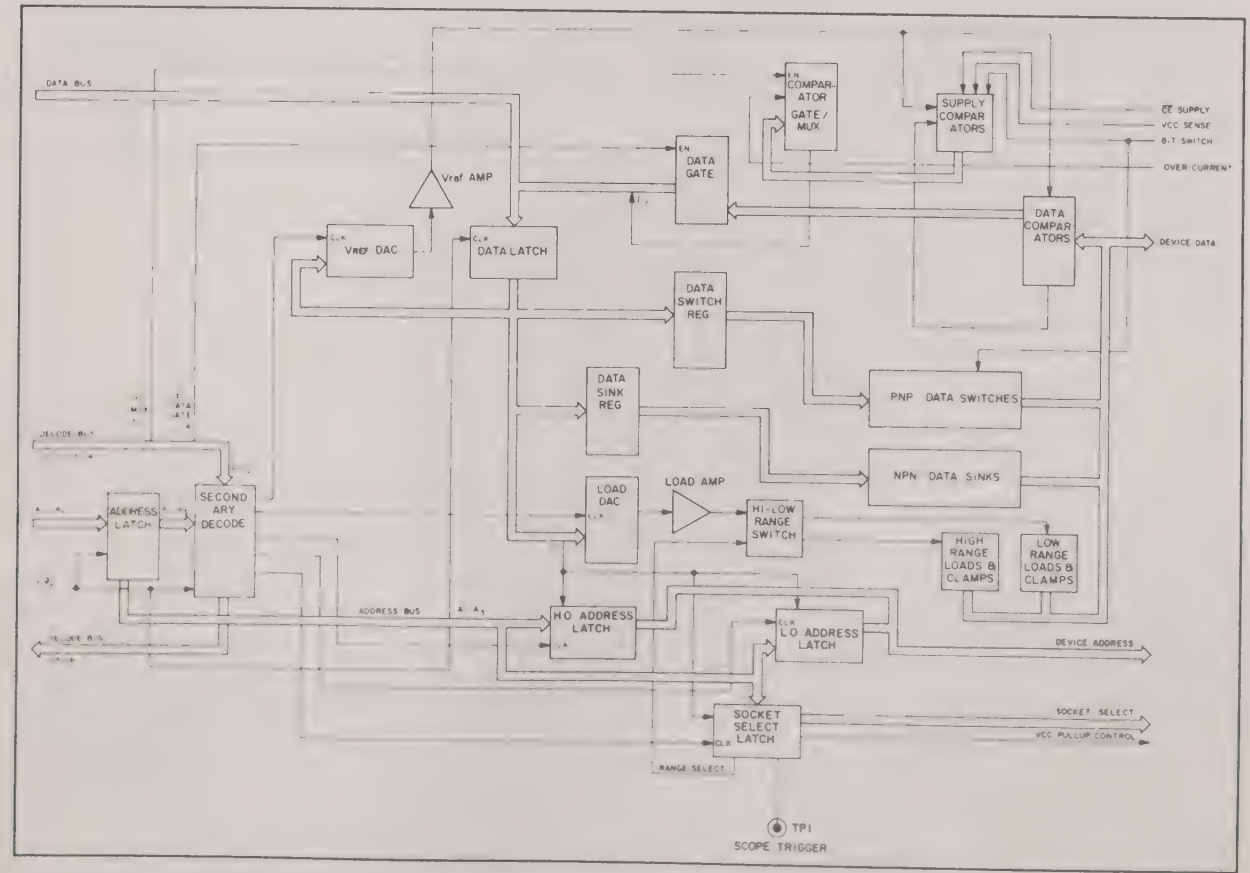

Figure 5-5. Block Diagram, Address and Data Driver Card

5.3.4 UniPak™ Socket Card

The UniPak™ socket card distributes to the device sockets the signals developed on the address and data driver card and the waveform generator. Refer to the block diagram, figure 5-6. The device address lines connect directly to the device sockets; larger devices connect to more device addresses than smaller devices; diode-overvoltage protection on these lines prevents damage to the drivers on the address and data driver card.

The device-data bus connects directly to all sockets. Four-bit devices are connected to PD_1-PD_4. The data pulldowns consist of 1K-ohm resistors and a diode network. Data-spike clamps consist of diode networks and capacitor-resistor networks. The diode networks are used to clip overshoot on the data-line programming pulses. The capacitor network is charged by the bit supply so that the network does not absorb energy from the actual data-line programming pulses.

Pins 18, 19, 20 and 21 of the 24-pin device socket receive signals directly from the waveform generator via the corresponding pin switches. A spike-suppression network similar to that used on the data lines is provided where the $\overline{CE}$ supply charges the RC network. V_{CC} is applied to all sockets through seven diodes. Remote sensing of the voltage at the selected socket is provided by the analog switch of the V_{CC}-sense multiplexer. When V_{CC} is brought to zero, the device's V_{CC} lines can be pulled up by the V_{CC} pullups. The V_{CC} sense-multiplexer and a comparator on the address and data driver card are then used to read the V_{CC} voltage. If a device is properly inserted in a socket, the V_{CC} voltage will be above 2V. If it is in backwards, it will be below 1V, and if no device is in the socket, the voltage will approach 4V.

The LED decoder is used to light the LEDs below the selected socket.

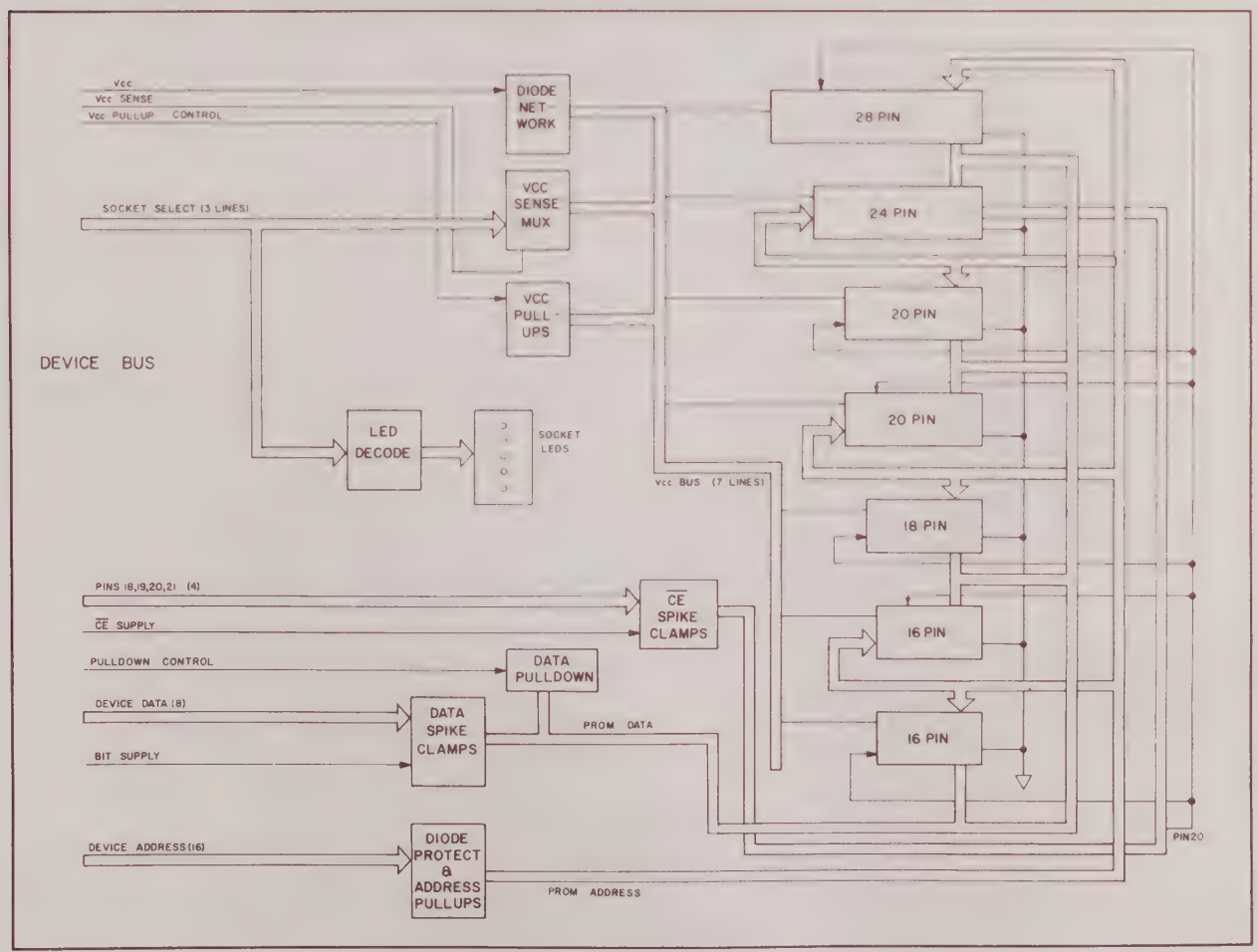

Figure 5-6. Block Diagram, UniPak™ Socket Card

5.3.5 UniPak™ Memory Card

The UniPak™ memory card is shown in block diagram form in figure 5-7. PROMs which store the UniPak™ software are contained on the memory card. These PROMs connect to the address bus directly and to the data bus through data buffers.

Two PROMs and a latch comprise the primary decoder. The PROMs connect to the 12 high-order address lines and the R/$\overline{W}$ line. Outputs from the primary-decoder latch connect to the secondary decoder and also to secondary decoders on the address and data driver card and the waveform generator. A 1-of-8 decoder, timed with $\overline{V \bullet \emptyset_2}$, provides the secondary decoding for the software PROMs. Two additional lines from this decoder connect to the address card to provide the decode signals for the data gate and comparator gate/multiplexer. Additional outputs from the primary decoder enable the data buffer during all software-read operations and lower the data-gate-enable line during any access of the UniPak™

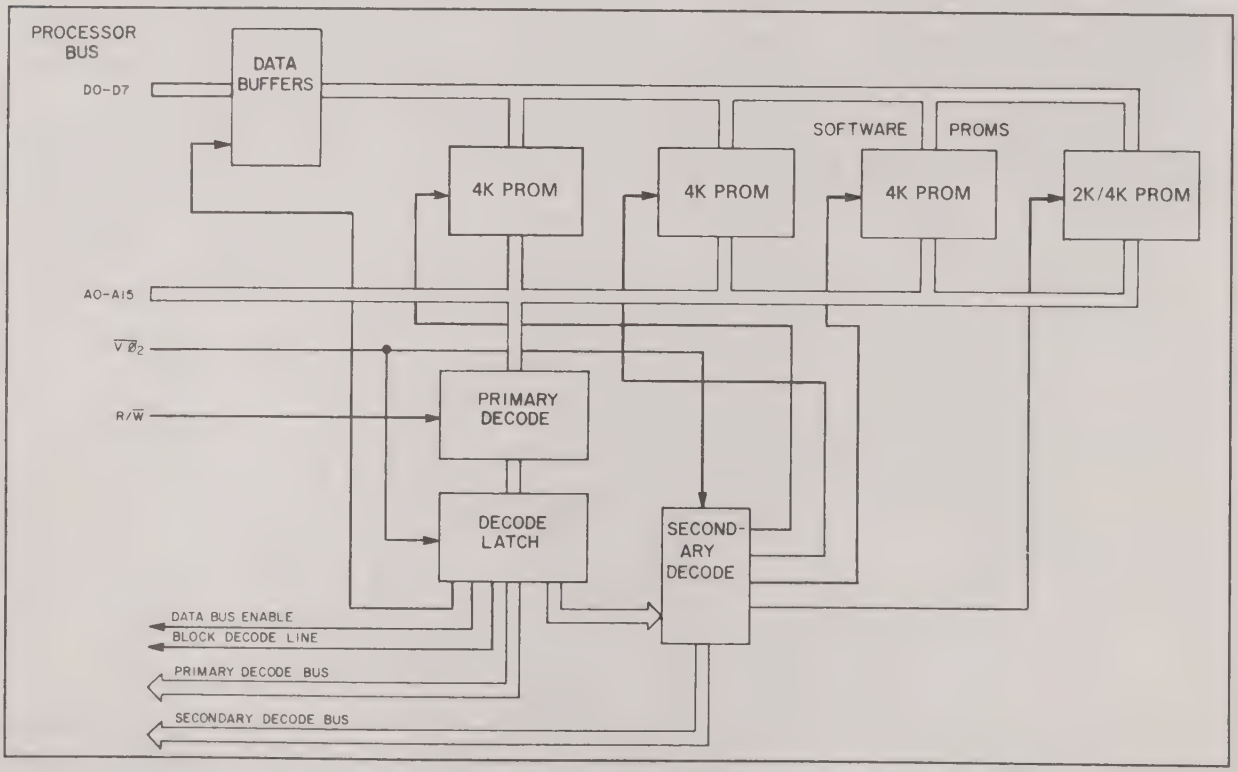

Figure 5-7. Block Diagram, UniPak™ Memory Card

APPENDIX A
ERROR CODES

CODE	NAME	DESCRIPTION
21	Illegal-Bit Error	The device cannot be programmed due to already programmed locations of incorrect polarity.
23	First-Pass Verify Error	The device data was incorrect on the first pass of the automatic verify sequence during device programming.
24	Second-Pass Verify Error	The device data was incorrect on the second pass of the automatic verify sequence during device programming.
27	Insufficient RAM	Due to the value of the Begin RAM Address, there is insufficient RAM to program the device, or the total allotment of RAM resident is less than the word limit of the device.
30	No Programming Algorithm	Valid family and pinout codes are not selected, or family code selection is not followed by pinout code selection.
31	Excessive Current Drain	The operation aborted due to excessive current drain by a device.
32	Backward Device	The operation aborted due to V_{CC} level test indicating a backward device.
35	Faulty Chip Select	The operation aborted due to data being present while a device is disabled.
37	Socketing Error	Operation aborted due to a low V_{CC} level indication on sockets presumed to be empty. A device may be in the wrong socket, or two or more devices may be socketed simultaneously.
38	Illegal Operation During Calibration	An illegal or invalid operation was attempted during calibration.
39	Failure to Lock Security Fuse	The security bit did not program and the device is not locked.
70	Faulty Bit Supply	The operation aborted due to a faulty bit supply. Do not use UniPak™ until repaired.
71	Faulty CS Supply	The operation aborted due to a faulty CS supply. Do not use UniPak™ until repaired.
72	Faulty V_{CC} Supply	The operation aborted due to a faulty V_{CC}. Do not use UniPak™ until repaired.
B0	Byte Erase Error	The device does not have a byte erase mode. Block limits must be removed and a chip erase performed. The entire chip may then be reprogrammed.
B1	Chip Erase Error	The device does not have a chip erase mode.

*In the case of an error condition, be sure that the family and pinout codes are correct for the PROM installed; refer to the UniPak Device List to cross check family and pinout codes.

UNIPAK™ DEVICE LIST

This document comes in two parts. The first is a list of the UniPak device family and pinout codes. An explanation of each of the column headings is given below. The second is a flow chart of the KEPROM™ algorithm.

CAUTION

Be sure you enter the proper family and pinout codes for the device you want to program. If you enter an incorrect family and pinout code, you may damage your device. Be aware that although you may enter an independently valid family code and an independently valid pinout code, when combined, produce an invalid (illegal) combination. The correct combination for your device is published in this table. All family/pinout combinations not contained in this table are considered "illegal." Data I/O assumes no responsibility or liability for results produced by entry of "illegal" family/pinout combinations.

Key to Headings and Footnotes:

Device Part Number: The number assigned by the device manufacturer.

Family/Pinout Code: A 2-digit hexadecimal number that designates the programming algorithm (family) followed by a 2-digit hexadecimal number used to differentiate device types based on pin assignment and array size (pinout).

Software Version: A number in this column specifies the earliest version of the UniPak that will program the device to the manufacturer's latest specifications.

Adapter: The model number of the adapter required to program the designated device.

Approval Status: The following is an explanation of the symbols used in this column:

A Written approval obtained.

O Device is obsolete and no longer in production. No approval can be obtained. Algorithm has been used and approved in previous Data I/O equipment.

S This algorithm is in the process of submittal for manufacturer approval. The algorithm has been tested by Data I/O or the manufacturer, but no representation as to yield level is made or implied.

* Devices marked with this symbol following the approval status symbol has extra programmable locations beyond the main array. Data is entered sequentially in RAM above the main array data. Consult the manufacturer's specifications for specific information.

\# Devices marked with this symbol following the approval status symbol have security bits. Use SELECT CODE C3 to set the programming flow for the security bits.

\+ Devices marked with this symbol following the approval status symbol are KEPROMs. Refer to the KEPROM flow chart.

† Devices marked with this symbol following the approval status sybol cannot be programmed using the System 19 or the Model 100A.

\## Devices marked with this symbol following the approval status symbol can only be programmed by the 29B with V04 or later.

** Devices marked with this symbol following the approval status symbol have extra programmable locations beyond the main array. Data is entered sequentially in RAM above the main array data. Consult the manufacturer's specifications for specific information. To program asynchronous to synchronous, put 01 at second RAM location above the main array. Enter 00 to not program asynchronous to synchronous.

KEPROM™ is a trademark of the Intel Corporation.

UNIPAK™ DEVICE LIST

Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
		Advanced Micro Devices			
2708	21	27	A	None	A
27128	AF	51	005	None	A
27128A	C1	51	V08	None	S
2716	19	23	A	None	A
2716B	C2	23	V11	None	S
27256	C1	32	V08	None	S
2732	19	24	A	None	A
2732A	27	24	005	None	A
2732B	C2	24	V11	None	S
27512	DD	A4	V08	None	S†
2764	AF	33	005	None	A
2764A	C1	33	V08	None	S
27LS18	16	02	K	None	S
27LS184	16	06	E	None	S
27LS185	16	06	E	None	S
27LS19	16	02	K	None	A
27PS181	16	37	K	None	A
27PS184	16	06	A	None	A
27PS185	16	06	K	None	A
27PS191	16	68	K	None	A
27PS281	16	37	003	None	S
27PS291	16	68	003	None	A
27PS41	16	53	005	351A-065	S
27PS43	16	63	004	None	A
27S08	15	02	A	None	O
27S09	15	02	A	None	O
27S10	15	01	A	None	O
27S11	15	01	A	None	O
27S12	16	03	A	None	A
27S13	16	03	A	None	A
27S15	16	79	005	351A-068	A
27S18	16	02	A	None	A
27S180	16	37	A	None	A
27S181	16	37	A	None	A
27S184	16	06	E	None	A
27S185	16	06	E	None	A
27S19	16	02	A	None	A
27S190	16	68	H	None	A
27S191	16	68	H	None	A
27S20	16	01	A	None	A
27S21	16	01	A	None	A
27S25	16	65	003	None	S
27S26	16	85	005	351A-067	A
27S27	16	85	005	351A-067	A
27S28	16	09	E	None	A
27S280	16	37	003	None	A
27S281	16	37	003	None	A
27S29	16	09	E	None	A

UNIPAK™ DEVICE LIST

Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Advanced Micro Devices (Continued)		
27S290	16	68	003	None	A
27S291	16	68	003	None	A
27S30	16	36	A	None	A
27S31	16	36	A	None	A
27S32	16	38	E	None	A
27S33	16	38	E	None	A
27S35	16	66	004	None	S
27S37	16	66	004	None	S
27S40	16	53	004	351A-065	A
27S41	16	53	004	351A-065	A
27S43	16	63	004	None	A
27S45	16	77	005	351A-066	A**
27S47	16	77	005	351A-066	A**
27S49	16	67	003	None	S
27S65	16	93	V08	351A-073	S*
27S75	16	94	V08	351A-073	S*
27S85	16	95	V08	351A-073	S*
2817A	BF	A2	V11	None	S
2864B	CA	A6	V11	None	S
29750A	16	02	A	None	O
29751A	16	02	A	None	O
29760A	16	01	A	None	O
29761A	16	01	A	None	O
29770	16	03	A	None	O
29771	16	03	A	None	O
29774	16	85	005	351A-067	S
29775	16	85	005	351A-067	O
8751H	54	58	V10	351A-071	S#
9864	C9	A6	V08	None	S
AM9708	21	27	A	None	A
AM9716	19	23	A	None	A
AM9732	19	24	A	None	A
AM9761	54	6A	V10	351A-071	S#
AM9764	AF	33	005	None	A
			ATMEL		
27256	93	32	V11	None	S
27C128	93	51	V11	None	S
27C256	93	32	V11	None	S
27C512	4B	A4	V11	None	S†
27C513	5B	5E	V11	None	S†
27C515	5B	CA	V11	None	S†
27C64	93	33	V11	None	S
27HC256	93	32	V11	None	S

UNIPAK™ DEVICE LIST

Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			ATMEL (Continued)		
27HC64	93	33	V11	None	S
27HC641	90	67	V11	None	S
27HC641L	90	67	V11	None	S
27HC642	90	67	V11	None	S
27HC642L	90	67	V11	None	S
28C04	C4	82	V11	None	S
28C16	C4	96	V11	None	S
28C17	C4	A2	V11	None	S
28C64	C4	98	V11	None	S
28HC16	C4	96	V11	None	S
28HC17	C4	A2	V11	None	S
			Electronic Arrays		
2708	21	27	A	None	O
2716	19	23	A	None	O
			Eurotechnique		
ET2716	19	23	005	None	A
ET2732	19	24	005	None	A
ET2764	35	33	V08	None	A
ETC2716	19	23	005	None	A
ETC2732	27	24	V11	None	S
			Exel Microelectronics Inc.		
2816A	B7	23	V08	None	S
2864A	C3	98	V10	None	S
2865A	C3	98	V11	None	S
46C15	CD	21	V11	None	S
46C16	CD	21	V10	None	S
			Fairchild		
2708	21	27	A	None	O
93417	01	01	A	None	A
93427	01	01	A	None	A
93436	01	03	A	None	A
93438	01	15	A	None	A
93446	01	03	A	None	A
93448	01	15	A	None	A
93450	01	16	A	None	A
93451	01	16	A	None	A
93452	01	05	A	None	A
93453	01	05	A	None	A
93510	01	21	004	None	A
93511	01	21	004	None	A
93L450	01	16	A	None	S
93L451	01	16	A	None	S

UNIPAK™ DEVICE LIST

Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Fujitsu		
27128	45	51	005	None	S
27128A	93	51	V11	None	S
27256	93	32	V11	None	S
2732	19	24	E	None	A
2732A	27	24	F	None	A
2764	45	33	005	None	S
27C128	45	51	005	None	S
27C256	45	32	V08	None	S
27C256A	93	32	V11	None	S
27C256H	93	32	V11	None	S
27C32A	27	24	A	None	S
27C512	4B	A4	V11	None	S†
27C64	45	33	005	None	S
28C64	C3	98	V11	None	S
28C65	C3	98	V11	None	S
8516	19	23	E	None	A
8518	21	27	E	None	A
8532	19	24	E	None	A
8742	50	57	005	351A-070	S
8749H	50	57	005	351A-070	S
			General Instruments		
27256	93	32	V11	None	S
27C128	93	51	V11	None	S
27C256	93	32	V11	None	S
27C512	4B	A4	V11	None	S†
27C513	5B	5E	V11	None	S†
27C515	5B	CA	V11	None	S†
27C64	93	33	V11	None	S
27HC64	93	33	V11	None	S
27HC641	90	67	V11	None	S
28C04	C4	82	V11	None	S
28C16	C4	96	V11	None	S
28C17	C4	A2	V11	None	S
28C64	C4	98	V11	None	S
28CP64	C4	98	V11	None	S
28HC16	C4	96	V11	None	S
28HC17	C4	A2	V11	None	S
5716	83	23	003	None	A
5816	37	23	003	None	S
			Harris		
6641	40	47	F	None	A@
7602	06	02	V10	None	S
7603	06	02	V10	None	S
7608	05	16	A	None	O

UNIPAK™ DEVICE LIST

Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Harris (Continued)		
7610	06	01	V10	None	S
7611	06	01	V10	None	S
7616	05	42	A	None	O
76160	05	21	A	None	O
76161	06	21	V10	None	S
76165	06	53	V10	351A-065	S
7620	06	03	V10	None	S
7621	06	03	V10	None	S
7629	05	43	A	None	O
76320	05	63	H	None	O
76321	06	63	V10	None	S
7640	06	15	V10	None	S
7641	06	15	V10	None	S
7642	06	05	V10	None	S
7642P	05	38	H	None	O
7643	06	05	V10	None	S
7643P	05	38	H	None	O
7644	05	04	A	None	O
7647R	05	79	V08	351A-068	S
7648	05	09	A	None	O
7649	06	09	V10	None	S
76641	06	67	V10	None	S
7680	05	16	A	None	O
7680RP	05	16	H	None	O
7681	06	16	V10	None	S
7681RP	05	16	H	None	O
7684	05	06	A	None	O
7684P	05	06	H	None	O
7685	06	06	V10	None	S
7685P	05	06	H	None	O
7686	05	10	A	None	A
7687	05	10	001	None	O
			Hitachi		
27256	93	32	V10	None	S
27512	4B	A4	V11	None	S†
27C256	93	32	V11	None	S
27C64	79	33	V10	None	A
462532	19	25	F	None	A
462716	19	23	F	None	A
462732	19	24	F	None	A
462732P	19	24	A	None	S
48016	33	23	V09	None	S
4827128	79	51	004	None	A
4827128P	79	51	V10	None	S
482732A	27	24	A	None	A
482764	79	33	004	None	A
58064	D7	98	V10	None	S

UNIPAK™ DEVICE LIST

Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Hughes		
3004-1	58	62	004	None	A
3004-2	58	61	004	None	A
3008	58	60	004	None	A
3104-1	58	62	004	None	S
3104-2	58	61	004	None	S
3108	58	60	004	None	S
			Intel		
2704	21	26	A	None	O
2708	21	27	A	None	O
27128	79	51	004	None	A
27128A	93	51	005	None	A
2716	19	23	A	None	A
27256	93	32	005	None	A
2732	19	24	A	None	A
2732A	27	24	A	None	A
2732B	93	24	V10	None	S
27512	4B	A4	V09	None	S†
27513	5B	5E	V10	None	S†
2758	19	22	A	None	O
2764	79	33	004	None	A
2764A	93	33	005	None	A
27C256	93	32	V10	None	A
27C64	93	33	V09	None	S
2815	85	23	005	None	S
2816	37	23	H	None	S
2816A	A5	96	V08	None	S
2817A	BF	A2	V08	None	S
2864A	CC	98	V11	None	S
8704	21	26	A	None	O
8708	21	27	A	None	O
8741	56	59	005	351A-070	S
8741A	56	59	005	351A-070	S
8742	50	57	005	351A-070	S
8744	53	58	005	351A-071	S
8748	52	56	005	351A-070	S
8748H	50	56	005	351A-070	S
8749H	50	57	005	351A-070	S
8751	53	58	005	351A-071	S
8751H	D5	58	V08	351A-071	S#
8755A	47	55	005	351A-072	S
87C256	5C	C8	V11	None	S
87C64	93	3A	V10	None	S
P27128A	5C	51	V11	None	S
P27256	5C	32	V11	None	S
P2732A	4D	24	V11	None	S
P27512	5E	A4	V11	None	S†
P2764A	5C	33	V11	None	S

UNIPAK™ DEVICE LIST

Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Intersil		
6716	59	64	004	None	A
			Mitsubishi		
2708	21	27	A	None	S
27128	79	51	004	None	S
2716	19	23	A	None	A
2732	19	24	A	None	A
2764	79	33	004	None	S
8748	52	56	V08	351A-070	S
			Monolithic Memories		
5300	11	01	D	None	A
	E5	01	V09	None	S
5301	11	01	D	None	A
	E5	01	V09	None	S
5305	11	03	D	None	A
	E5	03	V09	None	S
5306	11	03	D	None	A
	E5	03	V09	None	S
5308	11	08	D	None	A
	D1	08	V08	None	A
5309	11	08	D	None	A
	D1	08	V08	None	A
5330	29	02	A	None	A
	E7	02	V09	None	S
5331	29	02	A	None	A
	E7	02	V09	None	S
5335	11	14	D	None	A
	D1	14	V08	None	A
5336	11	14	D	None	A
	D1	14	V08	None	A
5340	11	15	D	None	A
	D1	15	V08	None	A
5340JS	11	15	D	None	S
	D1	15	V08	None	A
5341	11	15	D	None	A
	D1	15	V08	None	A
5341JS	11	15	D	None	S
	D1	15	V08	None	A
5348	11	09	D	None	A
	D1	09	V08	None	A
5349	11	09	D	None	A
	D1	09	V08	None	A

UNIPAK™ DEVICE LIST

Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Monolithic Memories (Continued)		
5352	11	05	D	None	A
	D1	05	V08	None	A
5353	11	05	D	None	A
	D1	05	V08	None	A
5380	11	16	D	None	A
	D1	16	V08	None	A
5380JS	11	16	D	None	S
	D1	16	V08	None	A
5381	11	16	D	None	A
	D1	16	V08	None	A
5381JS	11	16	D	None	S
	D1	16	V08	None	A
5388	11	06	D	None	A
	D1	06	V08	None	A
5389	11	06	D	None	A
	D1	06	V08	None	A
53D1641	B2	80	V08	351A-073	S
53DA1643	AA	87	V08	351A-073	S*
53DA441	AA	AC	V08	351A-073	S*
53DA442	AA	AC	V08	351A-073	S*
53DA841	AA	AD	V08	351A-073	S*
53LS140	18	01	004	None	S
53LS141	18	01	004	None	S
53LS1681	18	21	V11	None	S
53LS240	18	03	004	None	S
53LS241	18	03	004	None	S
53LS441	18	05	004	None	S
53PL1681	18	21	V08	None	S
53PS1681	18	21	005	None	S
53RA1681	18	A3	V08	None	S*
53RA441	18	07	004	None	S
53RA481	EC	65	V09	None	S
53RS1681	18	A3	V08	None	S*
53RS881	18	86	005	None	A*
53S080	18	02	004	None	O
53S081	18	02	004	None	O
53S140	18	01	004	None	S
53S141	18	01	004	None	S
53S1641	18	53	004	351A-065	A
53S1681	18	21	004	None	S
53S1681J	18	21	004	None	S
53S240	18	03	004	None	S
53S241	18	03	004	None	S
53S280	18	08	004	None	S
53S281	18	08	004	None	S
53S285	18	14	V11	None	S
53S3281	18	63	004	None	A
53S440	18	05	004	None	S

UNIPAK™ DEVICE LIST

Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Monolithic Memories (Continued)		
53S441	18	05	004	None	S
53S480	18	09	004	None	S
53S481	18	09	004	None	S
53S485	18	15	V11	None	S
53S6481	18	67	V10	None	S
53S840	18	06	004	None	S
53S841	18	06	004	None	S
53S880	18	16	V11	None	S
53S881	18	16	003	None	S
6300	11	01	D	None	A
	E5	01	V09	None	S
6301	11	01	D	None	A
	E5	01	V09	None	S
6305	11	03	D	None	A
	E5	03	V09	None	S
6306	11	03	D	None	A
	E5	03	V09	None	S
6308	11	08	D	None	A
	D1	08	V08	None	A
6309	11	08	D	None	A
	D1	08	V08	None	A
6330	29	02	A	None	A
	E7	02	V09	None	S
6331	29	02	A	None	A
	E7	02	V09	None	S
6335	11	14	D	None	A
	D1	14	V08	None	A
6336	11	14	D	None	A
	D1	14	V08	None	A
6340	11	15	D	None	A
	D1	15	V08	None	A
6340JS	11	15	D	None	S
	D1	15	V08	None	A
6341	11	15	D	None	A
	D1	15	V08	None	A
6341JS	11	15	D	None	S
	D1	15	V08	None	A
6348	11	09	D	None	A
	D1	09	V08	None	A
6349	11	09	D	None	A
	D1	09	V08	None	A
6352	11	05	D	None	A
	D1	05	V08	None	A
6353	11	05	D	None	A
	D1	05	V08	None	A
6380	11	16	D	None	A
	D1	16	V08	None	A
6380JS	11	16	D	None	S
	D1	16	V08	None	A

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Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Monolithic Memories (Continued)		
6381	11	16	D	None	A
	D1	16	V08	None	A
6381JS	11	16	D	None	S
	D1	16	V08	None	A
6388	11	06	D	None	A
	D1	06	V08	None	A
6389	11	06	D	None	A
	D1	06	V08	None	A
63D1641	B2	80	V08	351A-073	S
63D1642	B2	80	V08	351A-073	A
63DA1643	AA	87	V08	351A-073	S*
63DA441	AA	AC	V08	351A-073	S*
63DA442	AA	AC	V08	351A-073	S*
63DA841	AA	AD	V08	351A-073	S*
63LS140	18	01	004	None	S
63LS141	18	01	004	None	S
63LS1681	18	21	V11	None	S
63LS240	18	03	004	None	S
63LS241	18	03	004	None	S
63LS441	18	05	004	None	S
63PL1681	18	21	V08	None	S
63PS1681	18	21	005	None	S
63RA1681	18	A3	V08	None	S*
63RA441	18	07	004	None	S
63RA481	EC	65	V09	None	S
63RS1681	18	A3	V08	None	S*
63RS881	18	86	005	None	A*
63S080	18	02	004	None	A
63S081	18	02	004	None	A
63S140	18	01	004	None	S
63S141	18	01	004	None	S
63S1641	18	53	004	351A-065	A
63S1681	18	21	004	None	S
63S1681J	18	21	004	None	S
63S240	18	03	004	None	S
63S241	18	03	004	None	S
63S280	18	08	004	None	S
63S281	18	08	004	None	S
63S285	18	14	V11	None	S
63S3281	18	63	004	None	A
63S440	18	05	004	None	S
63S441	18	05	004	None	S
63S480	18	09	004	None	S
63S481	18	09	004	None	S
63S485	18	15	V11	None	S
63S6481	18	67	V10	None	S
63S840	18	06	004	None	S
63S841	18	06	004	None	S

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Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Monolithic Memories (Continued)		
63S880	18	16	V11	None	S
63S881	18	16	004	None	S
			Monolithic Memories (PLE)		
PLE5P8AC	18	02	V09	None	S
PLE5P8AM	18	02	V09	None	S
PLE5P8C	18	02	V09	None	S
PLE5P8M	18	02	V09	None	S
PLE8P4C	18	01	V09	None	S
PLE8P4M	18	01	V09	None	S
PLE8P8C	18	08	V09	None	S
PLE8P8M	18	08	V09	None	S
PLE9P4C	18	03	V09	None	S
PLE9P4M	18	03	V09	None	S
PLE9P8C	18	09	V09	None	S
PLE9P8M	18	09	V09	None	S
PLE9R8C	EC	65	V09	None	S
PLE9R8M	EC	65	V09	None	S
PLE10P4C	18	05	V09	None	S
PLE10P4M	18	05	V09	None	S
PLE10P8C	18	16	V09	None	S
PLE10P8M	18	16	V09	None	S
PLE10R8C	18	86	V09	None	S
PLE10R8M	18	86	V09	None	S
PLE11P4C	18	06	V09	None	S
PLE11P4M	18	06	V09	None	S
PLE11P8C	18	21	V09	None	S
PLE11P8M	18	21	V09	None	S
PLE11RA8C	18	A3	V09	None	S
PLE11RA8M	18	A3	V09	None	S
PLE11RS8C	18	A3	V09	None	S
PLE11RS8M	18	A3	V09	None	S
PLE12P4C	18	53	V09	351A-065	S
PLE12P4M	18	53	V09	351A-065	S
PLE12P8C	18	63	V09	None	S
PLE12P8M	18	63	V09	None	S
			Mostek		
2716	19	23	A	None	O
			Motorola		
67256C	49	32	V11	None	S
67259	49	32	V11	None	S
6836E16	2D	5A	V09	None	S
68732-0	25	44	A	None	O
68732-1	25	45	A	None	O
68769	25	29	V11	None	S
76161	05	21	A	None	S

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Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
		Motorola (Continued)			
76165	05	53	003	351A-065	S
7620	05	03	A	None	O
7621	05	03	A	None	S
7640	05	15	A	None	O
7641	05	15	A	None	S
7642	05	05	A	None	O
7643	05	05	A	None	S
7649	05	09	A	None	S
7680	05	16	A	None	O
7681	05	16	A	None	S
7684	05	06	A	None	O
7685	05	06	A	None	S
MCM2532	19	25	B	None	S
MCM2708P	21	27	A	None	O
MCM2716	19	23	B	None	S
MCM2808	81	72	003	None	S
MCM2816	43	23	003	None	S
MCM2817	81	71	003	None	S
MCM2832	81	70	003	None	S
MCM68708	21	27	A	None	A
MCM68764	25	29	V11	None	S
MCM68766	25	29	V11	None	S
TMS2716	23	28	A	None	O
		National Semiconductor			
2532	19	25	A	None	A
2708	21	27	A	None	A
2716	19	23	A	None	A
2732	19	24	A	None	A
2758A	19	22	A	None	A
2758B	19	35	A	None	A
27C128	5D	51	V10	None	S
27C16	19	23	E	None	A
27C16H	BD	23	V08	None	S
27C256	5D	32	V10	None	S
27C32	19	24	A	None	A
27C32B	5D	24	V11	None	S
27C32H	BD	24	V08	None	S
27C512	4C	A4	V10	None	S†
27C58A	19	22	A	None	S
27C58B	19	35	A	None	S
27C64	5D	33	V10	None	S
27CP128	5D	BB	V10	None	S
27CP256	4C	1E	V11	None	S
27CP64	5D	1D	V11	None	S

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Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
		National Semiconductor (Continued)			
2816	37	23	003	None	A
2864	C7	A5	V09	None	S
54LS471	08	08	A	None	O
54S188	08	02	A	None	O
54S287	08	01	A	None	O
54S288	08	02	A	None	O
54S387	08	01	A	None	O
54S471	08	08	K	None	O
54S472	08	09	A	None	O
54S473	08	09	A	None	O
54S474	08	15	A	None	A
54S475	08	15	A	None	A
54S570	08	03	A	None	O
54S571	08	03	A	None	O
54S572	08	05	A	None	O
54S573	08	05	A	None	O
54S574	08	34	A	None	O
74LS471	08	08	A	None	S
74S188	08	02	A	None	A
74S287	08	01	A	None	A
74S288	08	02	A	None	A
74S387	08	01	A	None	A
74S471	08	08	K	None	A
74S472	08	09	A	None	A
74S473	08	09	A	None	A
74S474	08	15	A	None	A
74S475	08	15	A	None	A
74S570	08	03	A	None	A
74S571	08	03	A	None	A
74S572	08	05	A	None	A
74S573	08	05	A	None	A
74S574	08	34	A	None	O
77LS181	08	16	A	None	A
77S180	08	16	A	None	A
77S181	08	16	A	None	A
77S184	08	06	A	None	A
77S185	08	06	A	None	A
77S190	08	21	A	None	A
77S191	08	21	A	None	A
77S195	08	53	004	351A-065	S
77S280	08	16	003	None	A
77S281	08	16	003	None	A
77S290	08	21	003	None	A
77S291	08	21	003	None	A
77S295	08	15	A	None	A
77S296	08	15	A	None	A
77S321	08	63	005	None	A
77SR181	08	66	V08	None	S*
77SR193	08	77	V11	365A-066	S

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Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			National Semiconductor (Continued)		
77SR25	08	65	V08	None	S*
77SR27	08	85	V09	351A-067	S
77SR474	08	81	V08	None	S*
77SR476	08	81	V10	None	S*
77X288	08	02	V10	None	S
87LS181	08	16	A	None	S
87S180	08	16	A	None	A
87S181	08	16	A	None	A
87S184	08	06	A	None	A
87S185	08	06	A	None	A
87S190	08	21	A	None	A
87S191	08	21	A	None	A
87S195	08	53	004	351A-065	S
87S280	08	16	003	None	A
87S281	08	16	003	None	A
87S290	08	21	003	None	A
87S291	08	21	003	None	A
87S295	08	15	A	None	A
87S296	08	15	A	None	A
87S321	08	63	005	None	A
87SR181	08	66	V08	None	S*
87SR193	08	77	V11	351A-066	S
87SR25	08	65	V08	None	S*
87SR27	08	85	V09	351A-067	S
87SR474	08	81	V08	None	S*
87SR476	08	81	V10	None	S*
87X288	08	02	V10	None	S
9716	B3	23	005	None	A
9816A	C3	96	V10	None	S
9817	BF	A2	V10	None	S
9817A	BF	A2	V10	None	S
98C64	9F	A7	V10	None	S
			Nippon Electric Company, Ltd.		
27128	79	51	004	None	S
2716	19	23	F	None	A
27256AD	48	32	V11	None	S
27256D	45	32	V11	None	S
2732	19	24	F	None	A
2732A	27	24	A	None	S
2764	79	33	004	None	A
27C64D	79	33	V11	None	S
27C256D	45	32	V11	None	A
8741AD	56	59	005	351A-070	S
8748	52	56	005	351A-070	S
8748AD	52	56	005	351A-070	S
8748H	50	56	005	351A-070	S
8749H	50	57	005	351A-070	S
8755A	47	55	005	351A-072	S

UNIPAK™ DEVICE LIST

Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Oki		
2708	21	27	A	None	A
27128	79	51	004	None	S
2716	19	23	A	None	A
2758	19	22	A	None	A
2764	79	33	004	None	S
8755A	47	55	005	351A-072	S
			Raytheon		
29600	11	08	D	None	A
29601	11	08	D	None	A
29602	11	08	D	None	A
29603	11	08	D	None	A
29610	11	03	D	None	A
29611	11	03	D	None	A
29612	11	03	D	None	A
29613	11	03	D	None	A
29620	11	09	D	None	A
29621	11	09	D	None	A
29622	11	09	D	None	A
29623	11	09	D	None	A
29624	11	15	D	None	A
29625	11	15	D	None	A
29626	11	15	D	None	A
29627	11	15	D	None	A
29630	11	16	D	None	A
29630SM	11	16	003	None	S
29631	11	16	D	None	A
29631SM	11	16	003	None	A
29632	11	16	D	None	A
29632SM	11	16	003	None	S
29633	11	16	D	None	A
29633SM	11	16	003	None	S
29634	11	16	D	None	A
29635	11	16	D	None	A
29636	11	16	D	None	A
29637	11	16	D	None	A
29640	11	53	004	351A-065	S
29641	11	53	004	351A-065	S
29642	11	53	004	351A-065	S
29643	11	53	004	351A-065	S
29650	11	06	D	None	A
29651	11	06	D	None	A
29652	11	06	D	None	A
29653	11	06	D	None	A
29660	11	01	D	None	A
29661	11	01	D	None	A
29662	11	01	D	None	A
29663	11	01	D	None	A

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Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Raytheon (Continued)		
29671	11	63	H	None	A
29673	11	63	H	None	A
29680	11	21	D	None	A
29680SM	11	21	003	None	S
29681	11	21	D	None	A
29681SM	11	21	003	None	S
29682	11	21	D	None	A
29682SM	11	21	003	None	S
29683	11	21	D	None	A
29683SM	11	21	003	None	S
29VP816	7A	68	V10	None	S
29VP832	7A	63	V10	None	S
29VP864	7A	67	V10	None	S
29VS816	7A	68	V10	None	S
29VS832	7A	63	V10	None	S
29VS864	7A	67	V10	None	S
39VP816	7A	68	V10	None	S
39VP832	7A	63	V10	None	S
39VP864	7A	67	V10	None	S
39VS816	7A	68	V10	None	S
39VS832	7A	63	V10	None	S
39VS864	7A	67	V10	None	S
			Ricoh		
27C256	93	32	V11	None	S
27C32	27	24	V11	None	S
27C64	79	33	V11	None	S
687C64	D9	29	V11	None	S
RD5H32	27	24	F	None	A
			Rockwell		
87C64	79	33	V10	None	S
			Samsung		
2816A	B7	23	V11	None	S
2864A	C3	98	V11	None	S
2865A	39	A6	V11	None	S
2817A	BF	A2	V11	None	S
2865AH	C9	A6	V11	None	S
			Seeq		
27128	79	51	005	None	S
2764	79	33	005	None	A
27C256	93	32	V08	None	S
2816A	B7	23	V08	None	S

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Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Seeq (Continued)		
2816AH	DF	23	V09	None	S
2817A	BF	A2	V08	None	S
2817AH	BF	A2	V08	None	S
2864H	C9	A6	V11	None	S
5133	79	33	005	None	A
5133H	79	33	005	None	A
5143	79	51	005	None	S
5213	A5	96	V08	None	S
5213H	B9	96	V08	None	S
52B13	A5	96	V08	None	S
52B13H	B9	96	V08	None	S
52B23	AB	97	V08	None	S
52B23H	F1	97	V09	None	S
52B33	AB	98	V08	None	S
52B33H	F1	98	V09	None	S
5516A	B7	23	V08	None	S
5516AH	DF	23	V09	None	S
5517A	BF	A2	V08	None	S
5517AH	BF	A2	V08	None	S
			SGS Technology		
2532	19	25	003	None	A
2716	19	23	003	None	A
27256	93	32	V11	None	S
2764	79	33	V08	None	S
2764A	93	33	V11	None	S
			Sharp		
LH764J	1D	33	V11	None	S
			Signetics		
2708	21	27	A	None	O
27C64	93	33	V08	None	S
27C256	93	32	V11	None	S
27C64A	93	33	V11	None	S
82123	10	02	V09	None	S
82LS135	10	08	A	None	S
82LS137	10	05	A	None	S
82LS180	10	16	A	None	A
82LS181	10	16	003	None	S
82PS180	10	16	V09	None	A
82PS181	10	16	003	None	S
82S114	AE	84	V10	351A-068	S
82S115	AE	83	V10	351A-068	S
82S123	10	02	A	None	A
82S126	10	01	A	None	A
82S129	10	01	A	None	A

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Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Signetics (Continued)		
82S130	10	03	A	None	A
82S131	10	03	V09	None	S
82S135	10	08	A	None	S
82S136	10	05	A	None	A
82S137	10	05	A	None	A
82S137A	0F	05	V11	None	S
82S140	10	15	A	None	A
82S141	10	15	A	None	A
82S146	10	09	A	None	A
82S147	10	09	A	None	A
82S180	10	16	A	None	A
82S181	10	16	A	None	A
82S182	10	16	A	None	A
82S183	10	16	A	None	A
82S184	10	06	A	None	A
82S185	10	06	A	None	A
82S190	10	21	A	None	A
82S191	10	21	A	None	A
82S195	10	53	004	351A-065	A
82S23	10	02	A	None	A
82S2708	10	16	A	None	A
82S321	10	63	004	None	A
			SMOS		
27128	79	51	V11	None	S
27C256	93	32	V11	None	S
27C64	79	33	V11	None	S
			Synertek		
2716	19	23	A	None	O
			Texas Instruments		
14S10	03	01	A	None	O
14SA10	03	01	A	None	O
18S030	04	02	A	None	A
18S22	04	08	A	None	O
18S42	04	09	A	None	O
18S46	04	15	A	None	O
18SA030	04	02	A	None	A
18SA22	04	08	A	None	O
18SA42	04	09	A	None	O
18SA46	04	15	A	None	O
24S10	13	01	A	None	A
24S166	13	53	005	351A-065	O

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Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Texas Instruments (Continued)		
24S41	13	38	A	None	A
24S81	13	06	A	None	A
24SA10	13	01	A	None	A
24SA166	13	53	005	351A-065	O
24SA41	13	38	A	None	A
24SA81	13	06	A	None	A
2508	19	22	A	None	A
2516	BD	23	V08	None	A
2532	BD	25	V08	None	A
2564	BD	30	V08	None	A
25L32	BD	25	V08	None	S
2708	21	27	A	None	A
27128	79	51	V08	None	A
27128A	93	51	V11	None	S
27256	93	32	V11	None	S
2732	BD	24	V08	None	A
2732A	63	24	V08	None	A
2764	79	33	V08	None	A
27C128	93	51	V11	None	A
27C256	93	32	V11	None	A
27L08	21	27	A	None	A
28L166	13	21	G	None	A
28L22	13	46	G	None	A
28L42	13	09	G	None	A
28L45	13	15	G	None	S
28L85	13	16	G	None	S
28L86	13	16	A	None	A
28LA22	13	46	G	None	A
28P166	13	21	G	None	S
28P42	13	09	G	None	S
28P45	13	15	G	None	S
28P85	13	16	G	None	S
28S166	13	21	G	None	A
28S2708	13	16	A	None	A
28S42	13	09	A	None	A
28S45	13	15	G	None	S
28S46	13	15	G	None	A
28S85	13	16	G	None	S
28S86	13	16	A	None	A
28SA166	13	21	G	None	S
28SA42	13	09	G	None	A
28SA46	13	15	G	None	A
28SA86	13	16	A	None	A
54LS2708	13	16	A	None	O
54LS478	13	16	A	None	O
54S188	04	02	A	None	O
54S2708	13	16	V09	None	O
54S287	03	01	A	None	O

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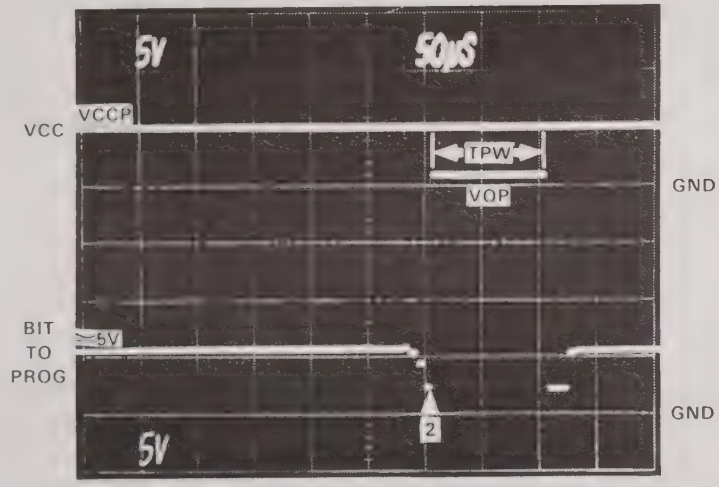
Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
			Texas Instruments (Continued)		
54S288	04	02	A	None	O
54S387	03	01	A	None	O
54S454	13	06	A	None	O
54S455	13	06	A	None	O
54S470	04	08	A	None	O
54S471	04	08	A	None	O
54S472	04	09	A	None	O
54S473	04	09	A	None	O
54S474	04	15	A	None	O
54S475	04	15	A	None	O
54S476	13	38	A	None	O
54S477	13	38	A	None	O
54S478	13	16	A	None	O
54S479	13	16	A	None	O
74188	04	02	A	None	O
74LS478	13	16	A	None	O
74S188	04	02	A	None	O
74S2708	13	16	A	None	O
74S287	03	01	A	None	O
74S288	04	02	A	None	O
74S387	03	01	A	None	O
74S454	13	06	A	None	O
74S455	13	06	A	None	O
74S470	04	08	A	None	O
74S471	04	08	A	None	O
74S472	04	09	A	None	O
74S473	04	09	A	None	O
74S474	04	15	A	None	O
74S475	04	15	A	None	O
74S476	13	38	A	None	O
74S477	13	38	A	None	O
74S478	13	16	A	None	O
74S479	13	16	A	None	O
TMS2716	23	28	A	None	O
			Thomson CSF		
27C64	93	33	V11	None	S
71190	92	21	004	None	A
71191	92	21	004	None	A
			Toshiba		
24128AP	5C	51	V11	None	S
24128P	79	51	V11	None	S
24256AP	5C	32	V11	None	S
24256P	45	32	V11	None	S

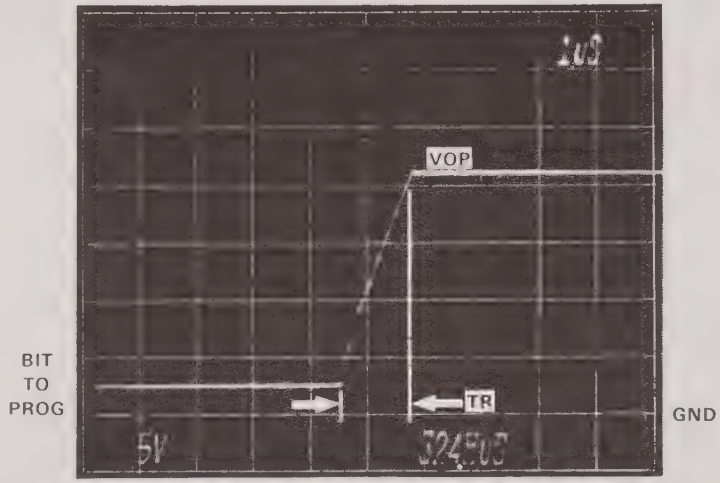
UNIPAK™ DEVICE LIST

Device Part Number	Family/Pinout Codes		Software Version	Adapter	Approval Status
		Toshiba (Continued)			
2464AP	5C	33	V11	None	S
2464P	79	33	V11	None	S
27128	79	51	004	None	S
27128AD	5C	51	V11	None	S
27256AD	5C	32	V11	None	S
2732	19	24	A	None	S
27512D	5E	A4	V11	None	S†
2764	79	33	004	None	S
2764AD	5C	33	V11	None	S
321	21	26	A	None	S
322	21	27	A	None	S
323	19	23	A	None	S
8755AC	47	55	005	351A-072	S
TC57256	45	32	V10	None	S
TMM27256	45	32	V10	None	S
		VLSI Technology, Inc.			
27C128	5D	51	V11	None	S
27C256	5D	32	V11	None	S
28H64	C9	A6	V10	None	S
VT27C512	4C	A4	V11	None	S†
VT27C64	5D	33	V11	None	S
		Waferscale Integration, Inc.			
WS27C128	3B	51	V11	None	S
WS27C256	3B	32	V11	None	S
WS27C64	3B	33	V11	None	S
WS57C128	3C	51	V11	None	S
WS57C256	3C	32	V11	None	S
WS57C49	3C	67	V11	None	S
WS57C64F	3C	33	V11	None	S
		Xicor			
2804A	B7	82	V08	None	S
2816A	B7	23	V08	None	S
2864A	C3	98	V11	None	S

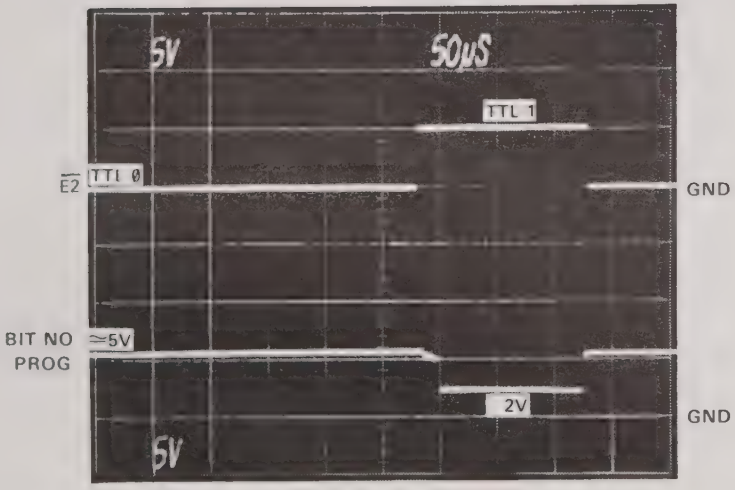
APPENDIX B
TIMING DIAGRAMS


5V
50µS
VCC
VCCP
TPW
VOP
GND
BIT
TO
PROG
≥5V
2
GND
5V

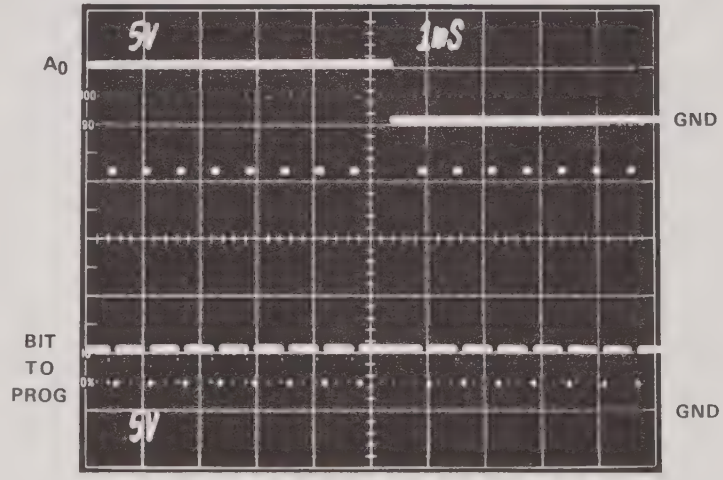
1


1µS
VOP
BIT
TO
PROG
TR
GND
5V

2


5V
50µS
TTL 1
E2
TTL 0
GND
BIT NO
PROG
≥5V
2V
GND
5V

3


5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	
	V_{OP}	20	20.5	21	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	90	100	110	us	
	t_r	0.5	1.0	3.0	us	
	Reject		8		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.3	4.4	4.5	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	6.4	7.4	8.4	V	701-1998/TP2
	LOW LOAD	6.4	7.4	8.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	4.9	5.0	5.1	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	6.4	7.4	8.4	V	701-1998/TP2
	LOW LOAD	6.4	7.4	8.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 01.*
2. *Load RAM with hex 01 for Family 02.*

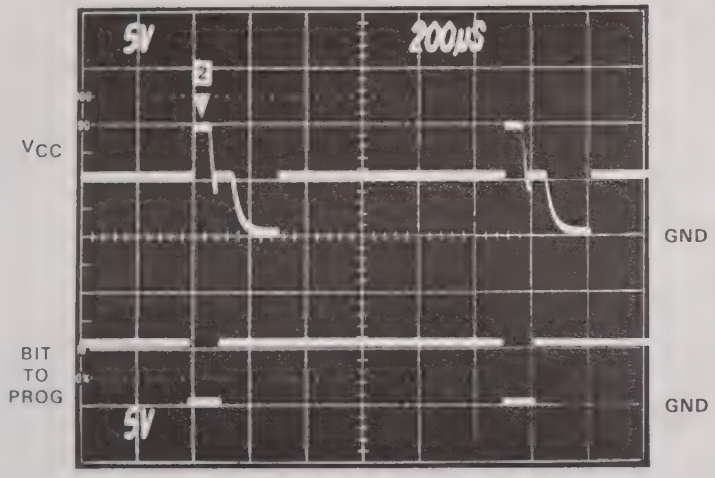
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

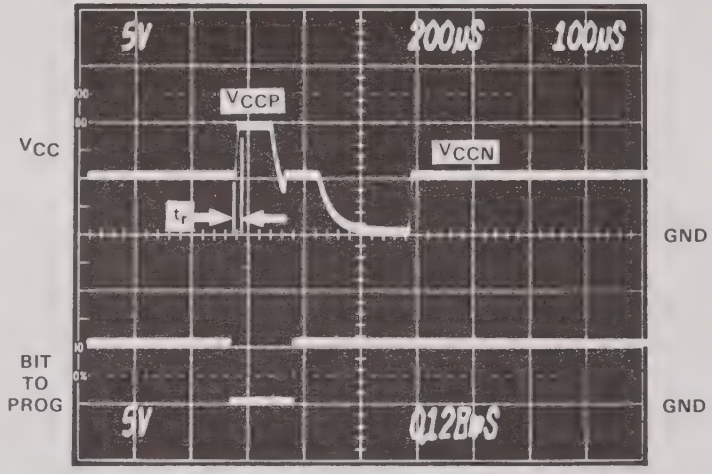
TIMING DIAGRAM

FAMILY CODES 01, 02

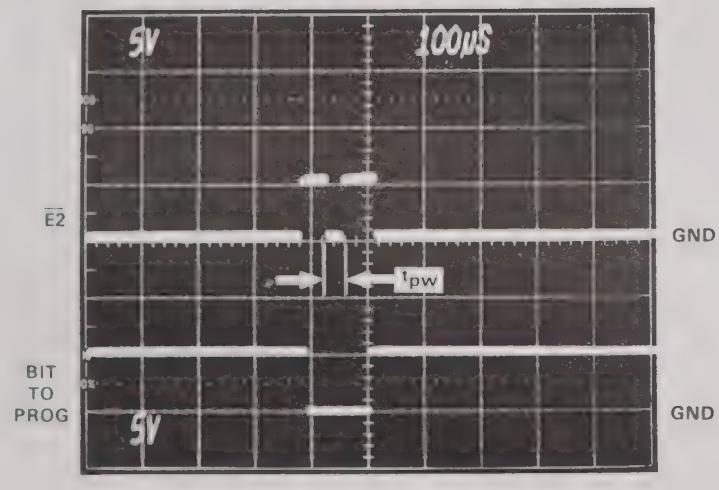
DATA I/O


5V
200µS
2
VCC
GND
BIT
TO
PROG
5V
GND

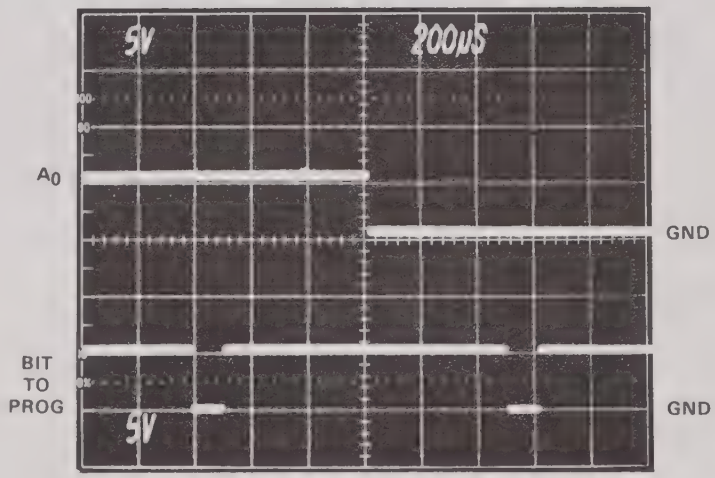
1


5V
200µS
100µS
VCCP
VCCN
VCC
tr
GND
BIT
TO
PROG
5V
GND

2


5V
100µS
E2
GND
tpw
BIT
TO
PROG
5V
GND

3


5V
200µS
A0
GND
BIT
TO
PROG
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	9.0	9.25	9.50	V	
	V_{OP}	0.0		0.3	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{CCN}	4.75	5.0	5.25	V	
	t_{pw}	15	25	110	us	
	t_r	5		20	us	
	Reject		1		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	10.6	11.6	12.6	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	1.6	1.7	1.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	8.4	9.4	10.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 03.*
2. *Load RAM with hex 01 for Family 04.*

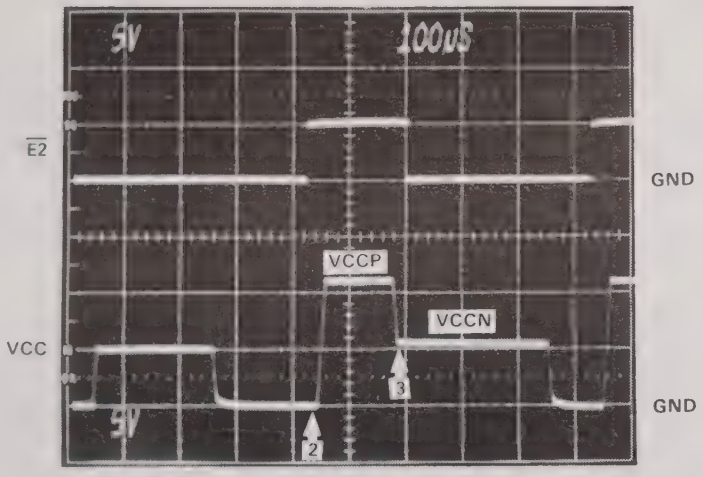
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

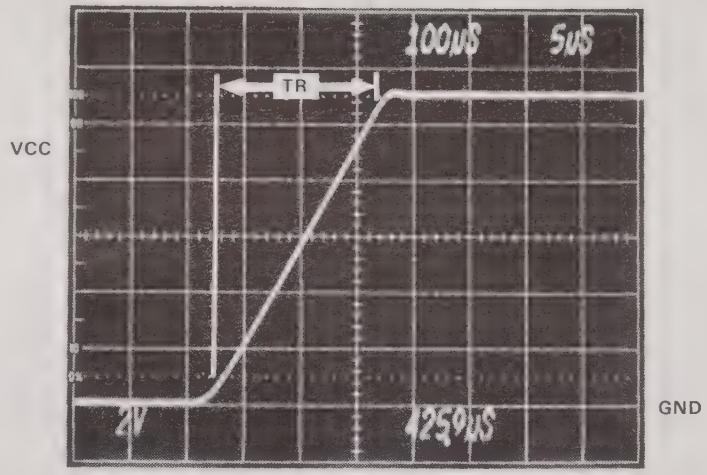
TIMING DIAGRAM

FAMILY CODES 03, 04

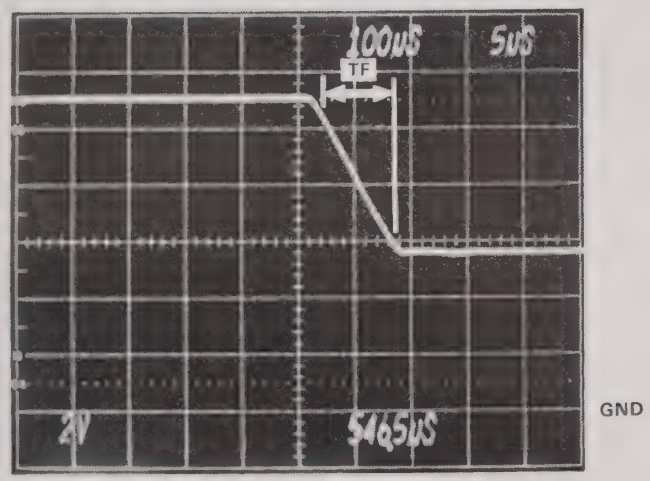
DATA I/O


5V
100uS
E2
GND
VCCP
VCCN
VCC
3
5V
2
GND

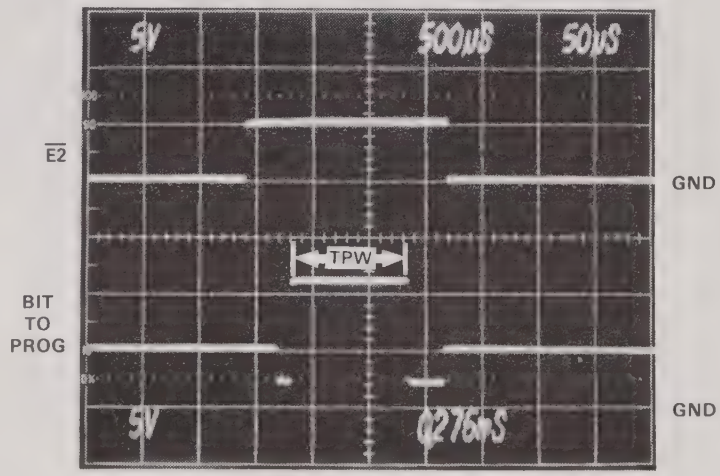
1


100uS
5uS
TR
VCC
2V
GND

2


100uS
5uS
TF
VCC
2V
GND

3


5V
500uS
50uS
E2
GND
TPW
BIT
TO
PROG
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	10.8	11.0	11.2	V	
	VCCN	5.3	5.5	5.7	V	
	VOP	10.5	11.0	11.5	V	
	TPW	90	100	110	μs	
	TR	17		31	μs	See Note 3
	TF	8		18	μs	See Note 3
	Reject		8		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.8	0.9	1.0	V	701-1998/TP4
	High Load	14.9	15.9	16.9	V	701-1998/TP2
	Low Load	14.9	15.9	16.9	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	1.6	1.7	1.8	V	701-1998/TP4
	High Load	11.9	12.9	13.9	V	701-1998/TP2
	Low Load	11.9	12.9	13.9	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 05.*
2. *Load RAM with hex 01 for Family 06.*
3. *Load VCC with a 100Ω, 2-watt resistor.*

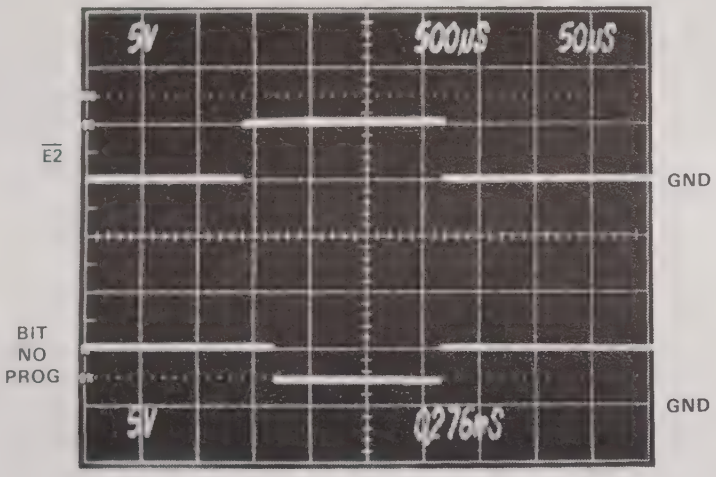
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

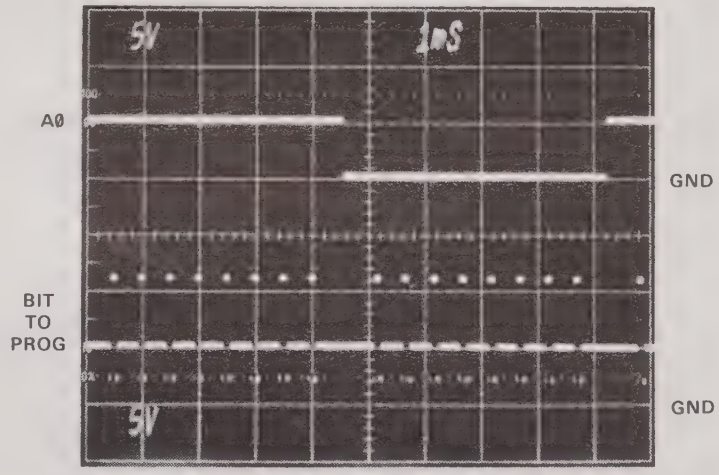
TIMING DIAGRAM

FAMILY CODES 05, 06

DATA I/O


5V
500uS
50uS
$\overline{E2}$
GND
BIT
NO
PROG
5V
GND

5


5V
1mS
A0
GND
BIT
TO
PROG
5V
GND

6

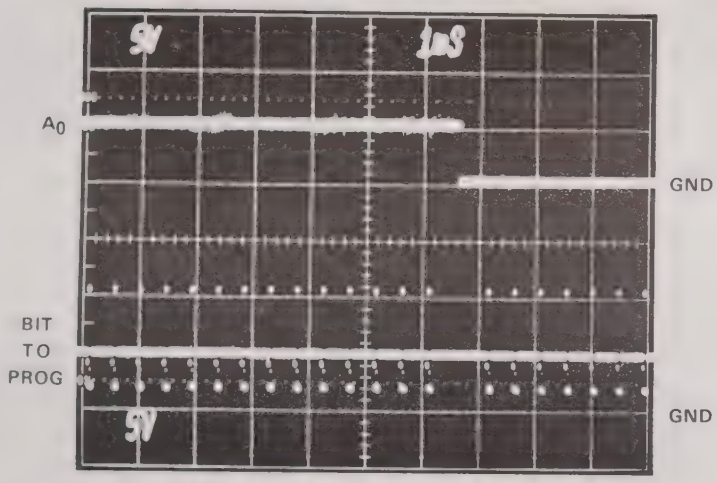
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

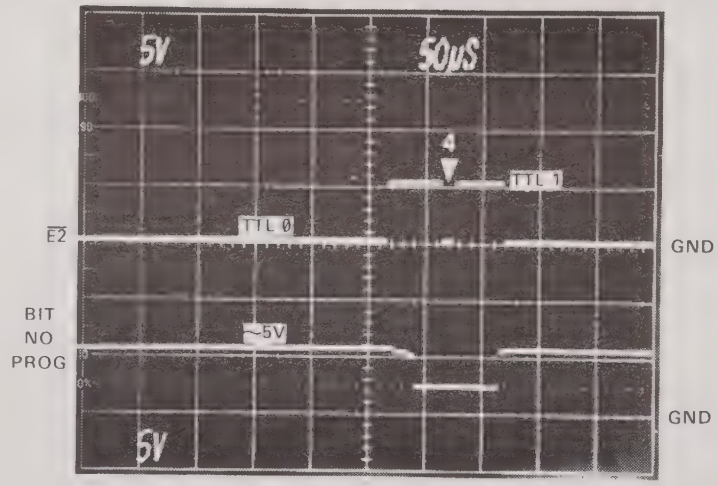
TIMING DIAGRAM

FAMILY CODES 05, 06

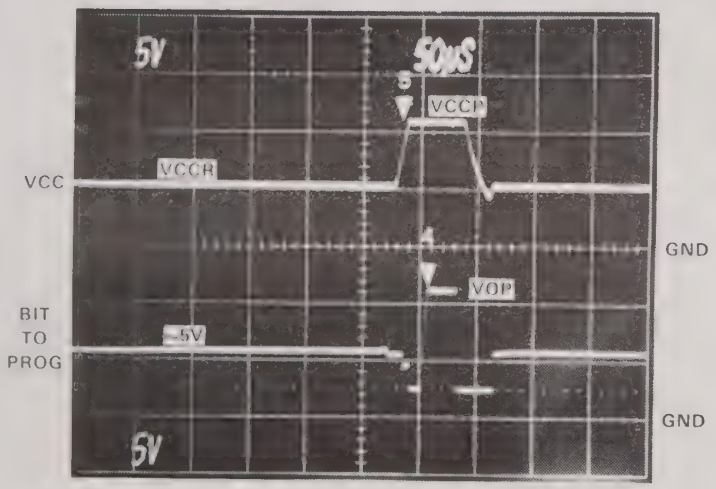
DATA I/O


5V
1μS
A0
GND
BIT
TO
PROG
GND
5V

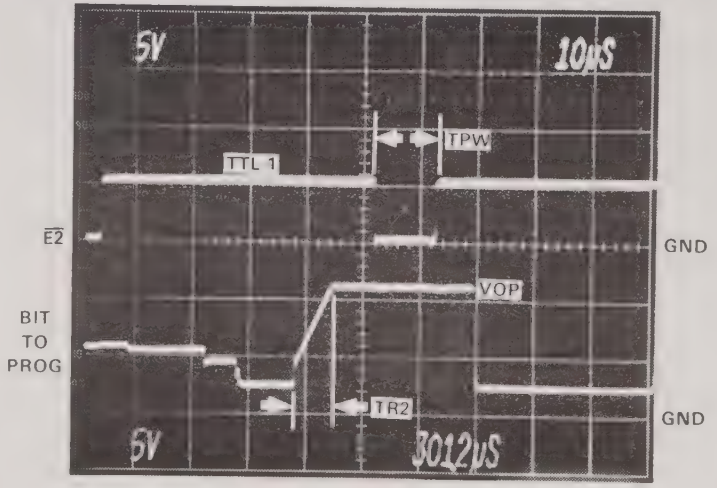
1


5V
50μS
4
TTL 1
TTL 0
E2
GND
BIT
NO
PROG
~5V
GND
5V

2


5V
50μS
5
VCCP
VCC
VCCR
GND
4
VOP
BIT
TO
PROG
~5V
GND
5V

3


5V
10μS
TPW
TTL 1
E2
GND
VOP
BIT
TO
PROG
TR2
GND
5V
3012μS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	10.0	10.5	11.0	V	
	V_{OP}	10.0	10.5	11.0	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{CCR}	4.75	5.0	5.25	V	
	t_{pw}	9	10	11	us	
	t_{r1}	1		25	us	
	t_{r2}	1		15	us	
	Reject		14		PULSES	
	Overprogram		5		PULSES	
1ST PASS VERIFY	V_{CC}	3.9	4.0	4.1	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	6.3	7.3	8.3	V	701-1998/TP2
	LOW LOAD	6.3	7.3	8.3	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	1.6	1.7	1.8	V	701-1998/TP4
	HIGH LOAD	5.4	6.4	7.4	V	701-1998/TP2
	LOW LOAD	5.4	6.4	7.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 07.*
2. *Load RAM with hex 01 for Family 08.*

REVISIONS

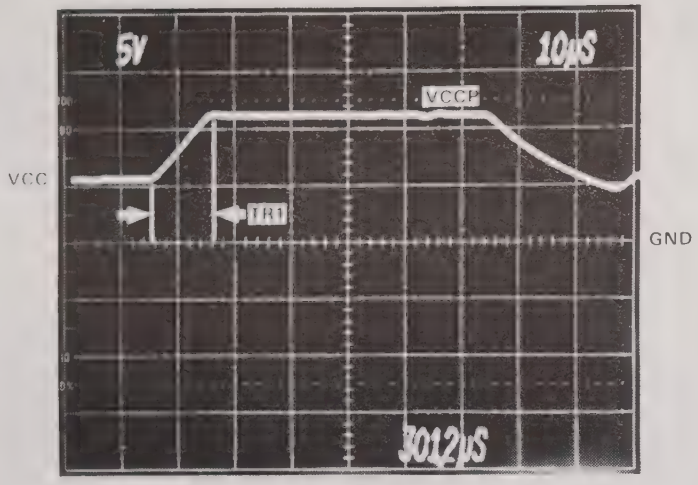
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022		

Sheet 1 of 2

TIMING DIAGRAM

FAMILY CODES 07, 08

DATA I/O



5

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

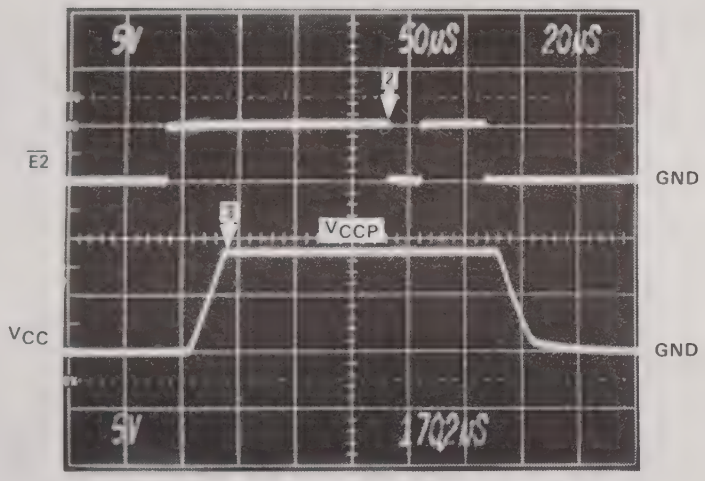
Sheet 2 of 2

TIMING DIAGRAM

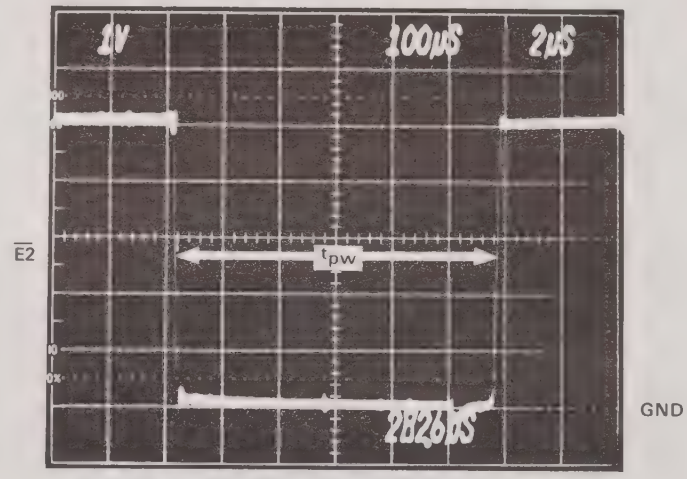
FAMILY CODES 07, 08

DATA I/O

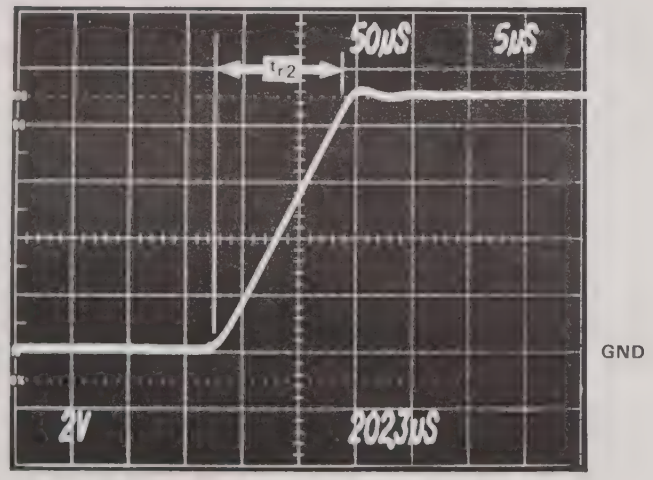
0526/1282


5V
50uS
20uS
$\overline{E2}$
GND
V_{CCP}
V_{CC}
GND
5V
1702uS

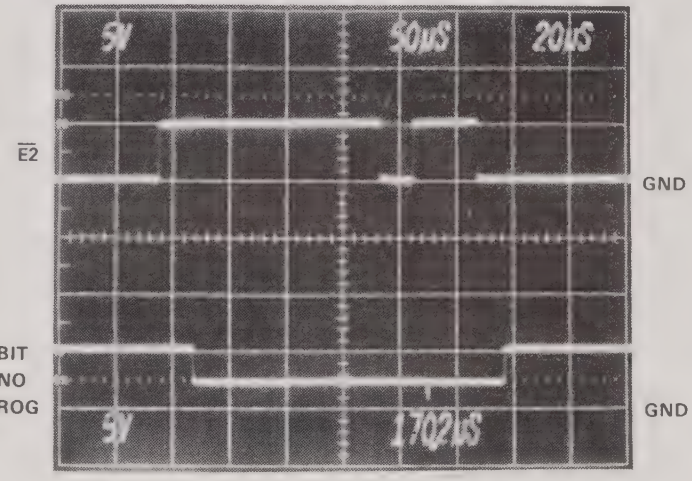
1


1V
100uS
2uS
$\overline{E2}$
t_{pw}
GND
2826uS

2


50uS
5uS
t_{r2}
V_{CC}
GND
2V
2023uS

3


5V
50uS
20uS
$\overline{E2}$
GND
BIT
NO
PROG
GND
5V
1702uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	8.5		9.0	V	
	V_{OP}	17.0	17.5	18.0	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	10		15	μs	
	t_{r1}	15		30	μs	
	t_{r2}	5		25	μs	See Note 3
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	1.4	1.5	1.6	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.7	5.2	5.5	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	1.4	1.5	1.6	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.7	5.2	5.5	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 09.*
2. *Load RAM with hex 01 for Family 10.*
3. *Load V_{CC} with a 100Ω, 2-watt resistor.*

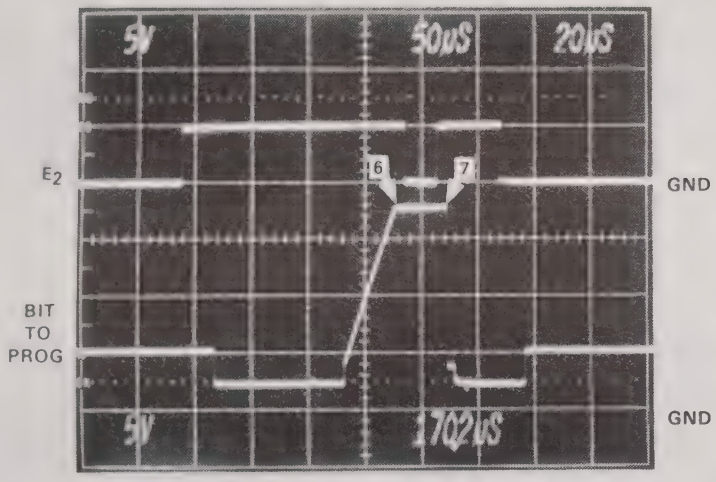
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

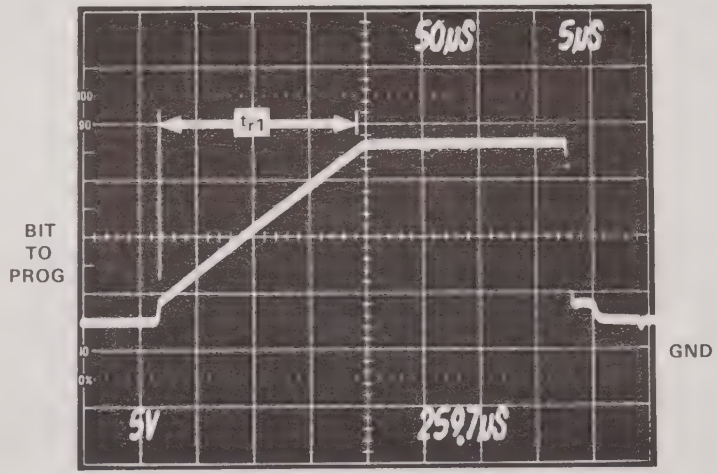
TIMING DIAGRAM

FAMILY CODES 09, 10

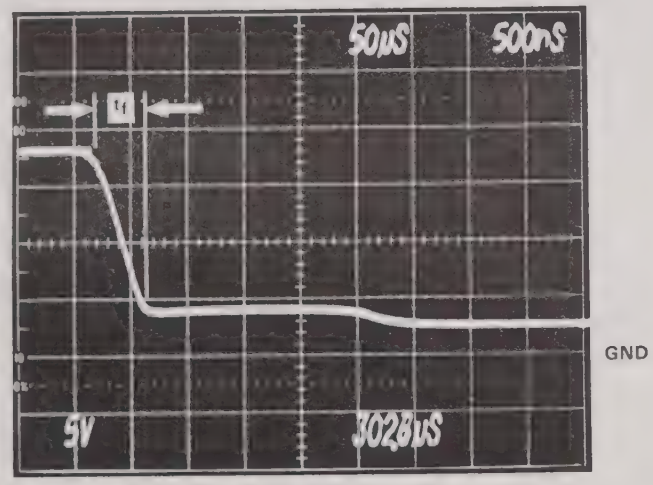
DATA I/O


5V
50uS
20uS
E2
16
7
GND
BIT
TO
PROG
5V
170.2uS
GND

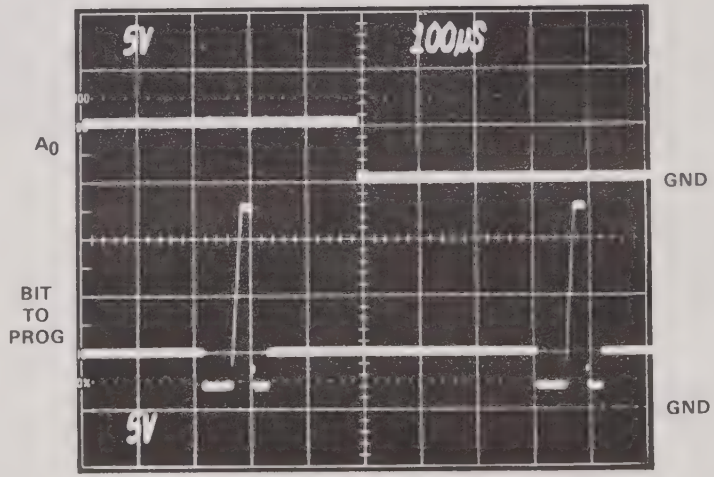
5


50uS
5uS
tr1
BIT
TO
PROG
GND
5V
259.7uS

6


50uS
500nS
tf
BIT
TO
PROG
GND
5V
302.8uS

7


5V
100uS
A0
GND
BIT
TO
PROG
GND
5V

8

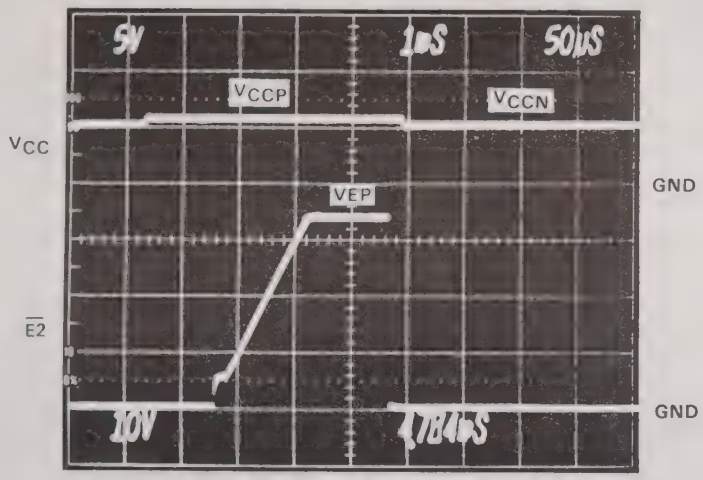
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

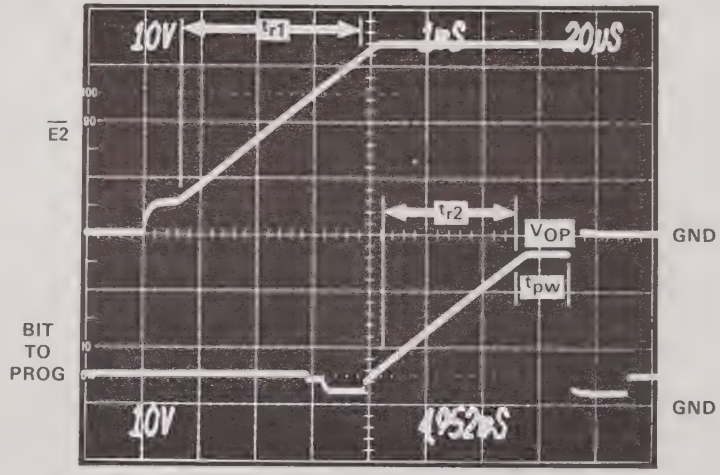
TIMING DIAGRAM

FAMILY CODES 09, 10

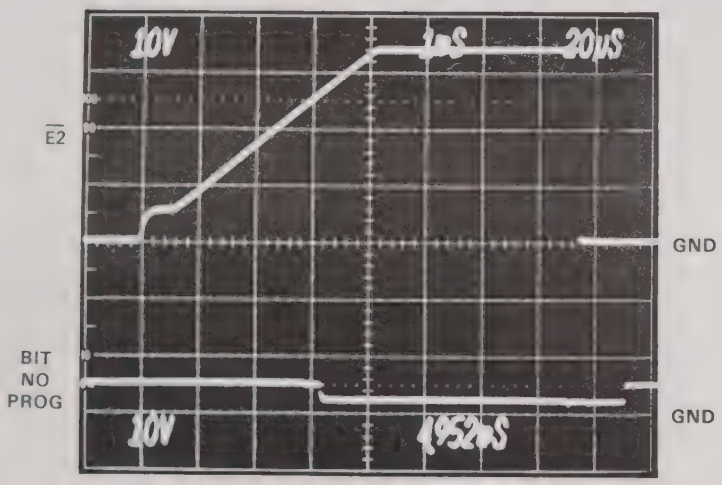
DATA I/O


5V
1mS
50µS
VCCP
VCCN
VCC
VEP
E2
GND
GND
10V
1.764mS

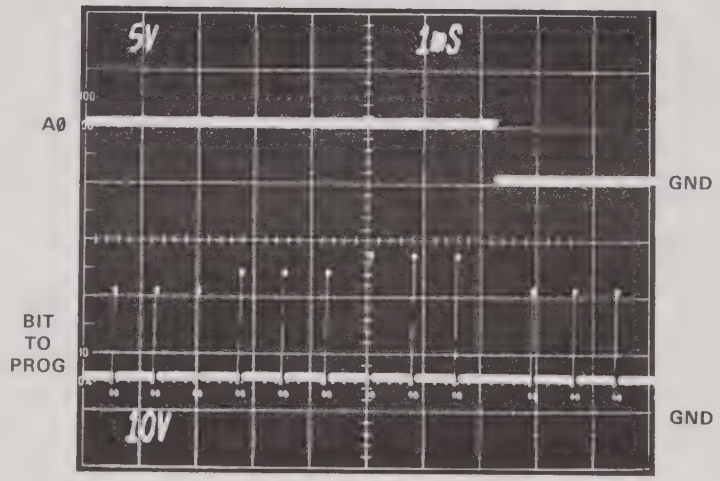
1


10V
tr1
1mS
20µS
E2
tr2
VOP
GND
tpw
BIT
TO
PROG
GND
10V
4.952mS

2


10V
1mS
20µS
E2
GND
BIT
NO
PROG
GND
10V
4.952mS

3


5V
1mS
A0
GND
BIT
TO
PROG
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCR}	4.75	5.0	5.25	V	
	V_{CCP}	5.4	5.5	5.6	V	
	V_{EP}	26	27	28	V	Pulses 1-3
		29	30	31	V	Pulses 4-6
		32	33	34	V	Pulses 7-9
	V_{OP}	19	20	21	V	Pulses 1-3
		22	23	24	V	Pulses 4-6
		25	26	27	V	Pulses 7-9
	t_{pw}	10		40	μs	See Note 3
	t_r	0.34	0.4	0.46	V/μs	
	t_{pp}	30		100	μs	
	Reject		9		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.1	4.2	4.3	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	17.3	18.3	19.3	V	701-1998/TP2
	LOW LOAD	17.3	18.3	19.3	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	2.9	3.0	3.1	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	5.2	5.7	6.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 11*
2. *Load RAM with hex 01 for Family 12.*
3. *This is measured at the 90% level of the pulse, and all three pulse levels must meet this specification.*

REVISIONS

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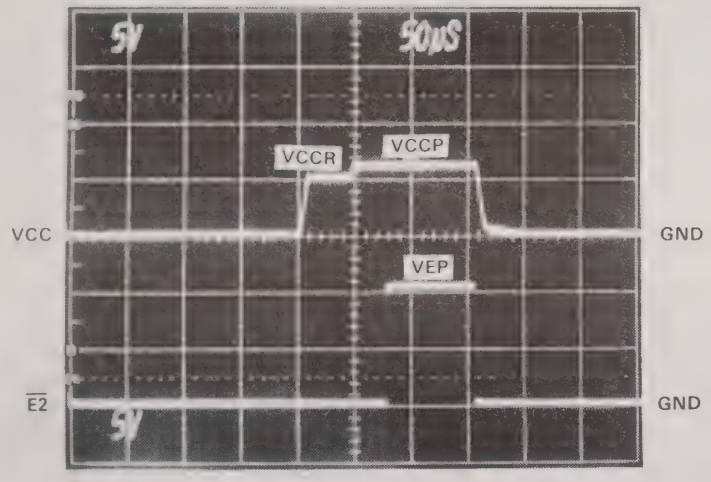
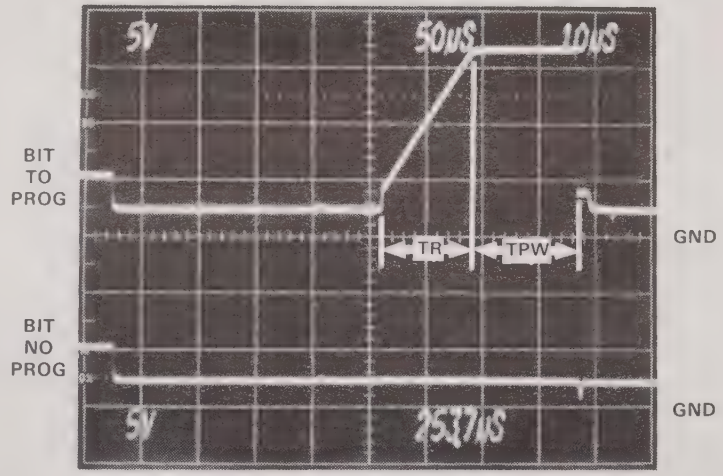
TIMING DIAGRAM

FAMILY CODES 11, 12

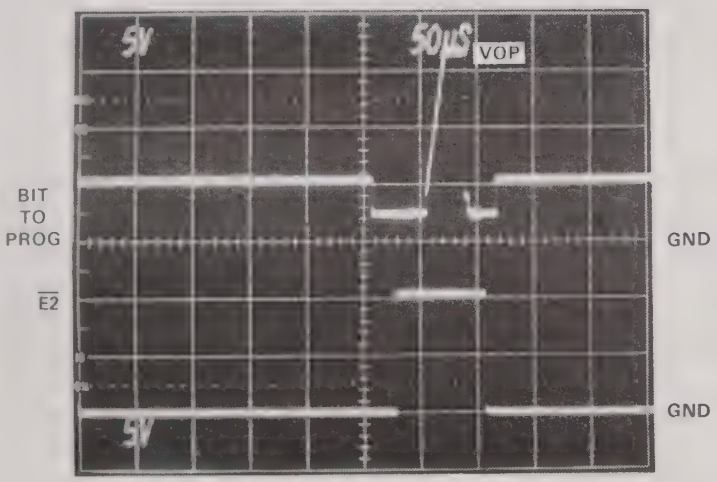
DATA I/O


5V
50µS
VCCR
VCCP
VCC
GND
VEP
E2
GND
5V

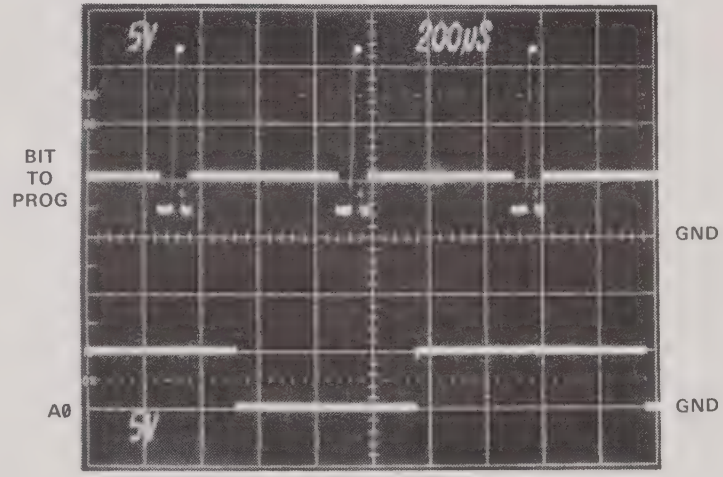
1


5V
50µS
10µS
BIT
TO
PROG
TR
TPW
GND
BIT
NO
PROG
GND
5V
253.7µS

2


5V
50µS
VOP
BIT
TO
PROG
GND
E2
GND
5V

3


5V
200µS
BIT
TO
PROG
GND
A0
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	
	V_{OP}	15.75	16.0	16.25	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{CCR}	4.75	5.0	5.25	V	
	V_{EP}	9.75	10.0	11.0	V	
	t_{pw}	15		20	us	
	t_r	10	15	20	us	
	Reject		1		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	0.9	1.0	1.1	V	701-1998/TP4
	HIGH LOAD	15.7	16.7	17.7	V	701-1998/TP2
	LOW LOAD	15.7	16.7	17.7	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	2.9	3.0	3.1	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	12.7	13.7	14.7	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 13.*
2. *Load RAM with hex 01 for Family 14.*
3. *Load V_{CC} with a 100Ω, 2-watt resistor.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

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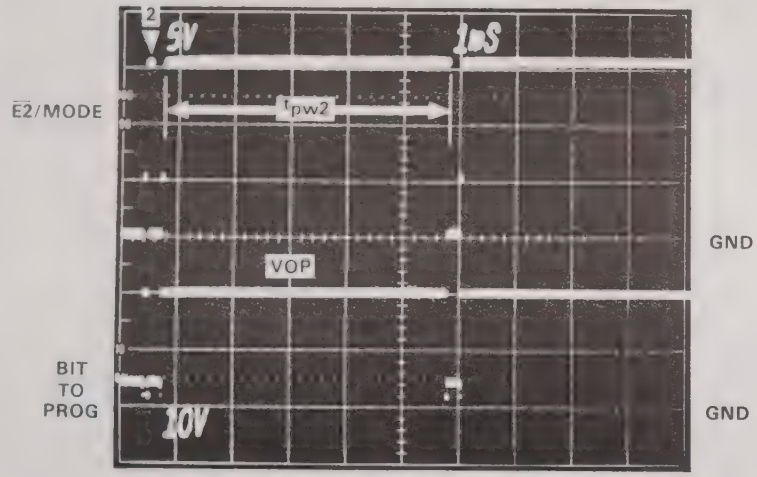
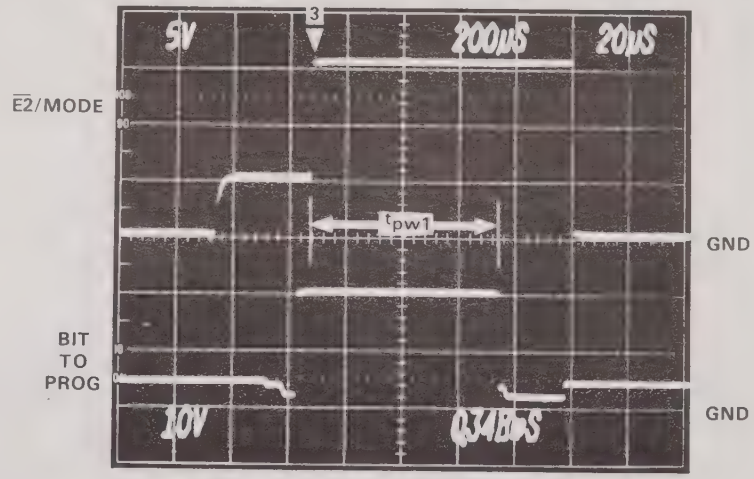
TIMING DIAGRAM

FAMILY CODES 13, 14

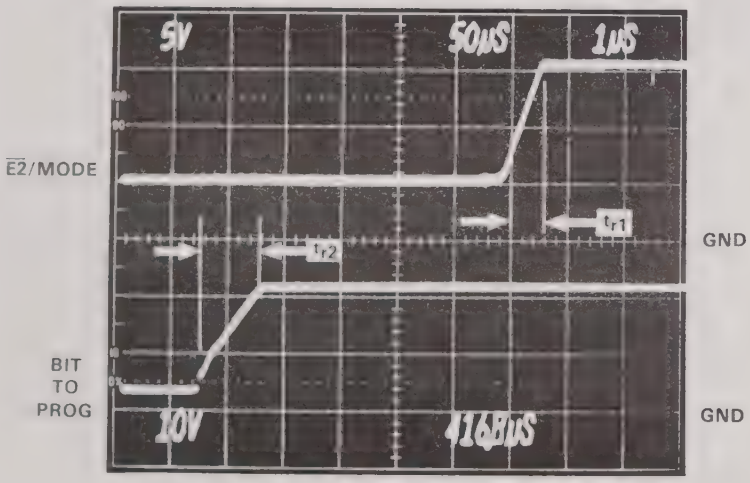
DATA I/O


2
5V
1μS
E2/MODE
tpw2
VOP
GND
BIT
TO
PROG
10V
GND

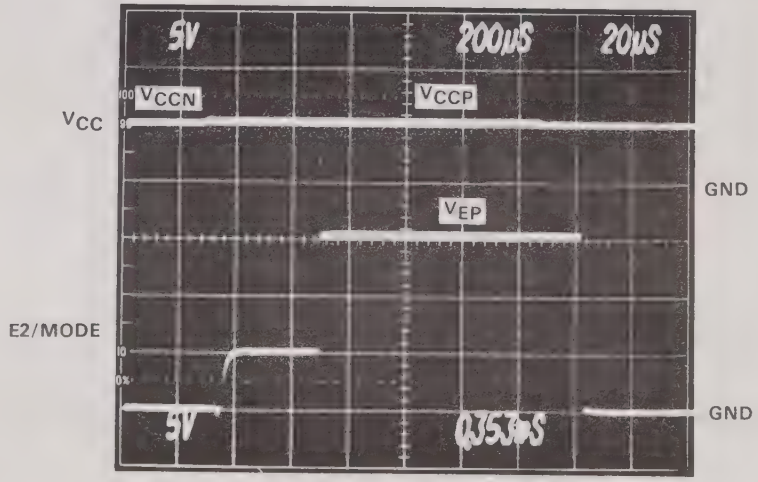
1


5V
3
200μS
20μS
E2/MODE
tpw1
GND
BIT
TO
PROG
10V
GND

2


5V
50μS
1μS
E2/MODE
tr1
tr2
GND
BIT
TO
PROG
10V
GND

3


5V
200μS
20μS
VCC
VCCN
VCCP
GND
VEP
E2/MODE
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCN}	4.75	5.0	5.75	V	
	V_{CCP}	5.0	5.25	5.5	V	
	V_{OP}	19.5	20.0	20.5	V	
	V_{EP}	14.5	15.0	15.5	V	
	t_{pw1}	50		100	us	Pulse 1
	t_{pw2}	5.0		15.0	ms	Pulse 2-80
	t_{r1}	.2		.7	us	
	t_{r2}	.6		1.4	us	
	Reject		80		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.6	4.7	4.8	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	23.7	24.7	25.7	V	701-1998/TP2
	LOW LOAD	23.7	24.7	25.7	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	18.1	19.1	20.1	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 15.*
2. *Load RAM with hex 01 for Family 16.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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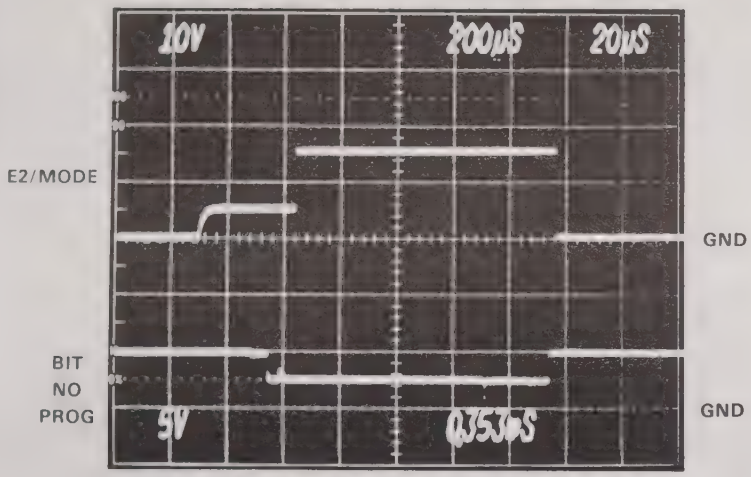
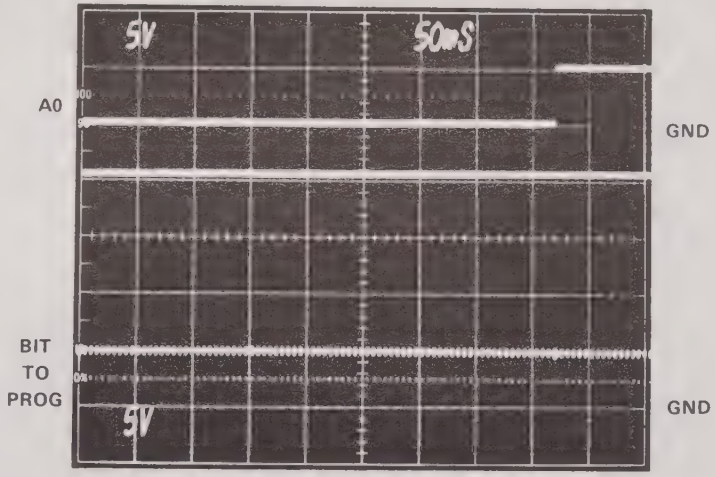
TIMING DIAGRAM

FAMILY CODES 15, 16

DATA I/O


10V
200µS
20µS
E2/MODE
GND
BIT
NO
PROG
5V
GND

5


5V
50mS
A0
GND
BIT
TO
PROG
5V
GND

6

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

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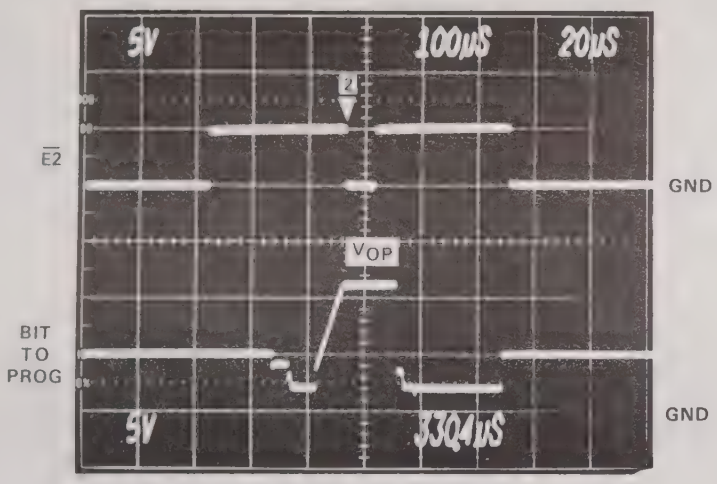
TIMING DIAGRAM

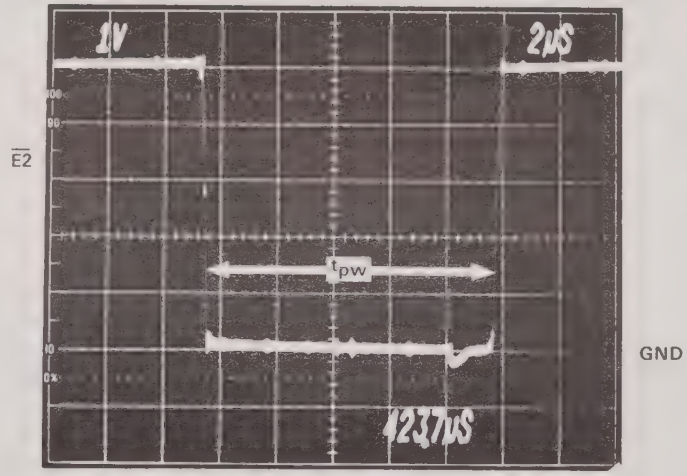
FAMILY CODES 15, 16

DATA I/O

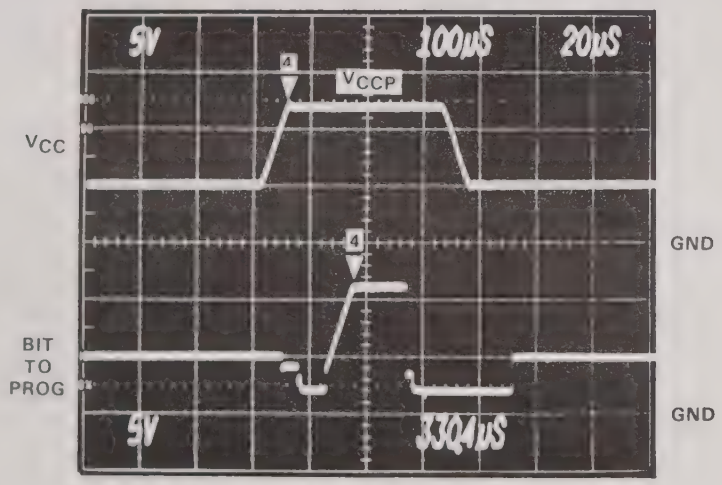
0526/1282


5V
100µS
20µS
2
$\overline{E2}$
GND
V_{OP}
BIT
TO
PROG
5V
3304µS
GND

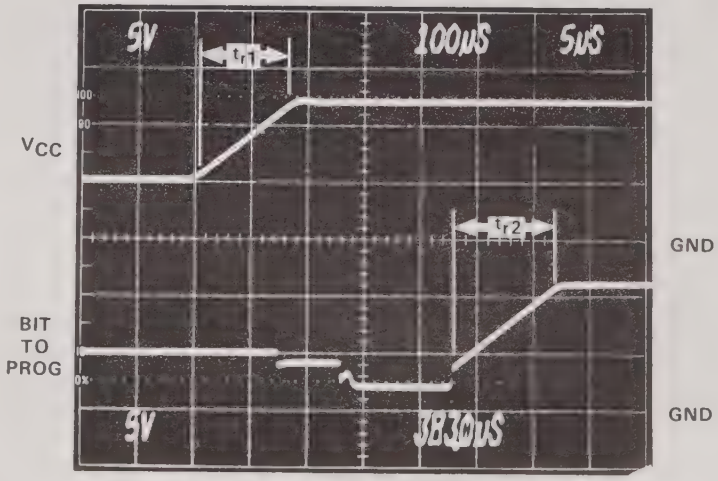
1


1V
2µS
$\overline{E2}$
t_{pw}
GND
1237µS

2


5V
100µS
20µS
4
V_{CCP}
V_{CC}
4
GND
BIT
TO
PROG
5V
3304µS
GND

3


5V
t_{r1}
100µS
5µS
V_{CC}
t_{r2}
GND
BIT
TO
PROG
5V
3830µS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	11.5	11.7	12.0	V	
	V_{OP}	10.5	11.0	11.5	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{CCN}	4.75	5.00	5.25	V	
	t_{pw}	9	10	11	us	
	t_{r1}	1		20	us	See Note 3
	t_{r2}	1		15	us	
	Reject		10		Pulses	
	Overprogram		5		Pulses	
1ST PASS VERIFY	V_{CC}	4.2	4.3	4.4	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	6.4	7.4	8.4	V	701-1998/TP2
	LOW LOAD	6.4	7.4	8.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	2.9	3.0	3.1	V	701-1998/TP4
	HIGH LOAD	7.2	8.2	9.2	V	701-1998/TP2
	LOW LOAD	7.2	8.2	9.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 17.*
2. *Load RAM with hex 01 for Family 18.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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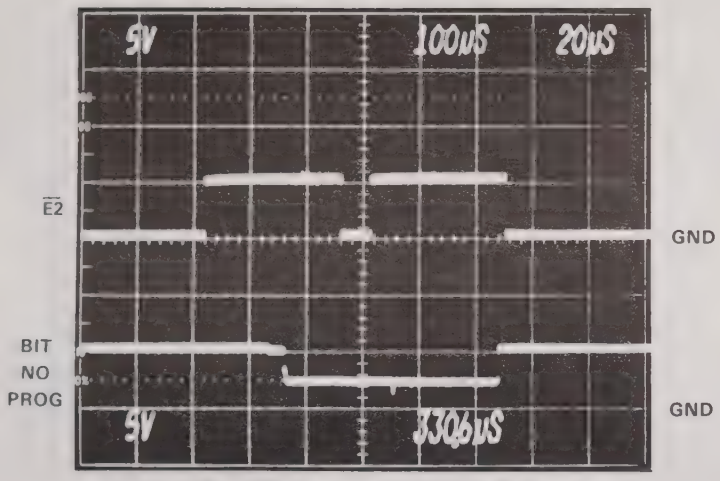
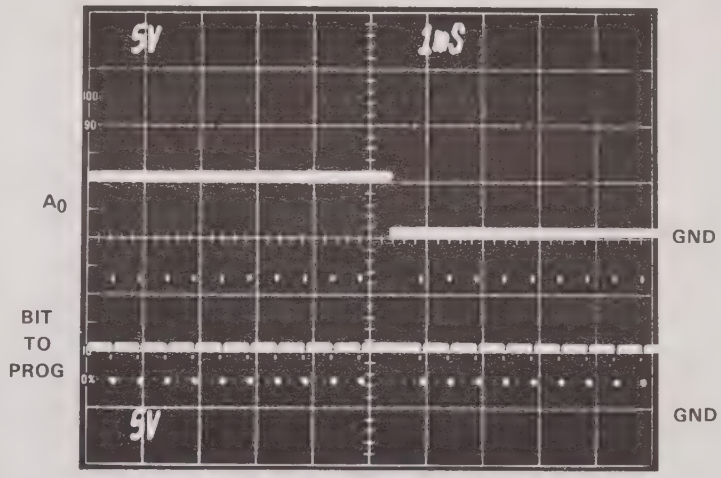
TIMING DIAGRAM

FAMILY CODES 17, 18

DATA I/O


5V
100uS
20uS
$\overline{E2}$
GND
BIT
NO
PROG
GND
5V
330uS

5


5V
1mS
A_0
GND
BIT
TO
PROG
GND
5V

6

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.00	5.25	V	
	VPPV	0.0	0.0	0.8	V	Pinout 24
	TPW	48	50	52	ms	
	T_R	50			ns	
	T_F	50			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 19.*
2. *Load RAM with hex 01 for Family 20, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photos 11 and 12 are for Pinout 24.*
4. *Photos 13 and 14 are for Pinout 25.*
5. *Photo 15 is for Pinout 49, using the same setup as photo 12.*
6. *Photo 16 is for Pinout 50, using the same setup as photo 14.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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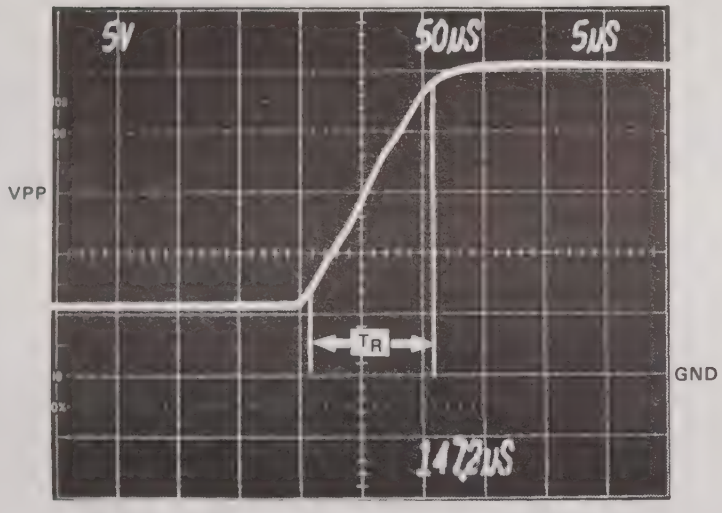
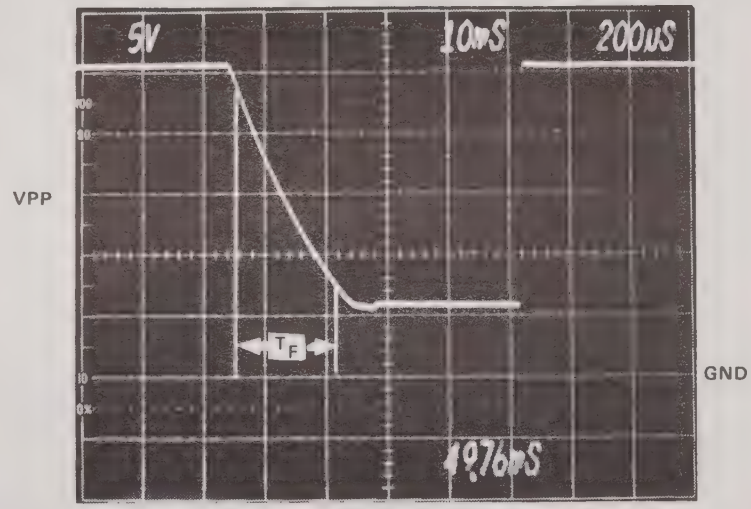
TIMING DIAGRAM

FAMILY CODES 19, 20

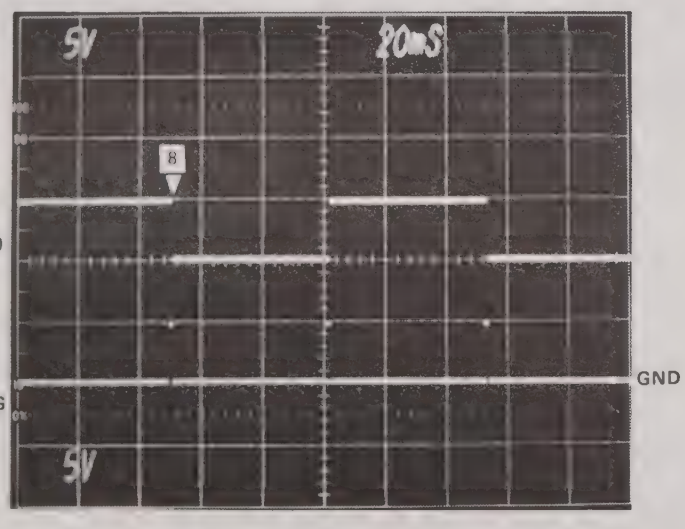
DATA I/O


5V
50uS
5uS
VPP
GND
T_R
147.2uS

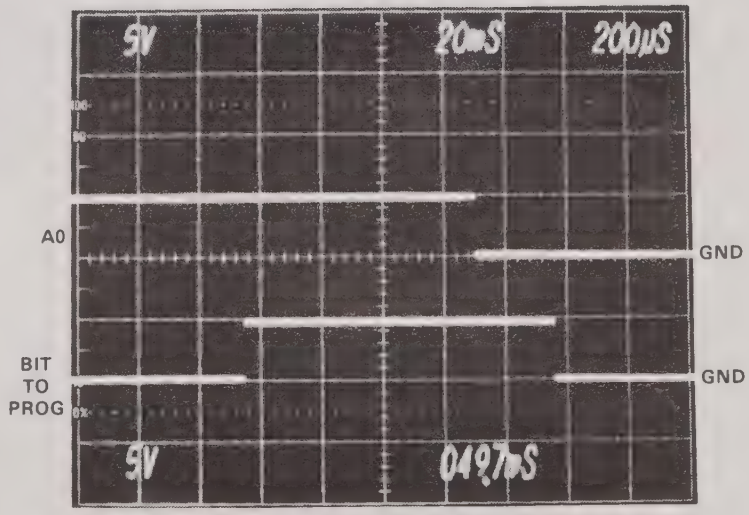
5


5V
10mS
200uS
VPP
GND
T_F
19.76mS

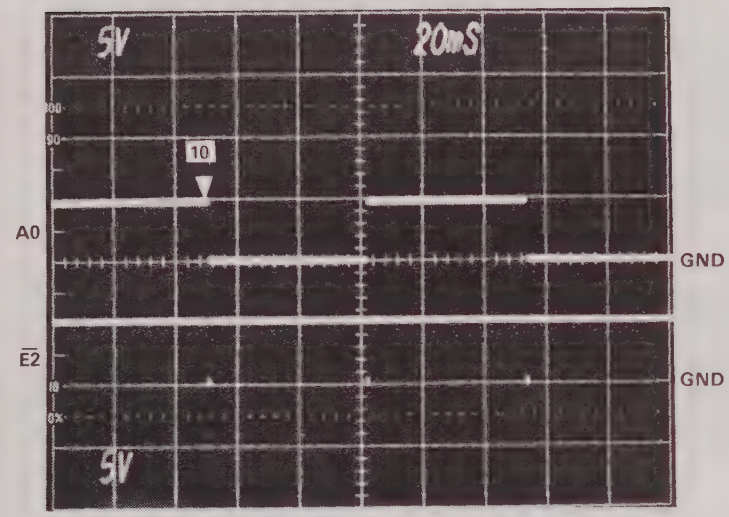
6


5V
20mS
B
A0
BIT
TO
PROG
GND
5V

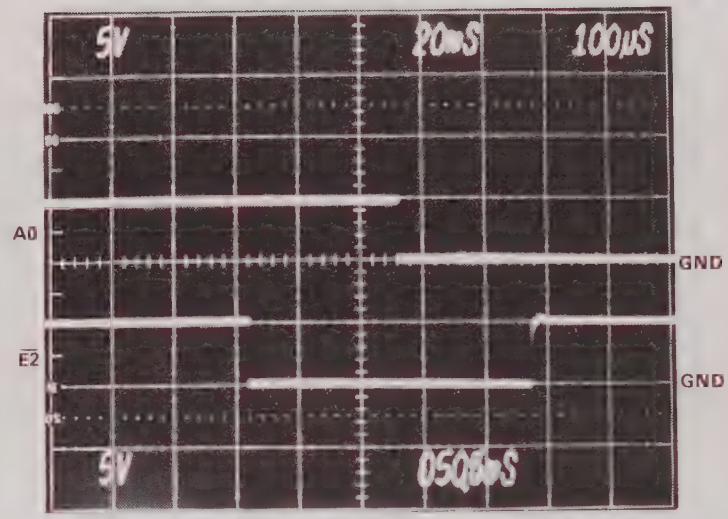
7


5V
20mS
200uS
A0
GND
BIT
TO
PROG
GND
5V
049.7mS

8



9



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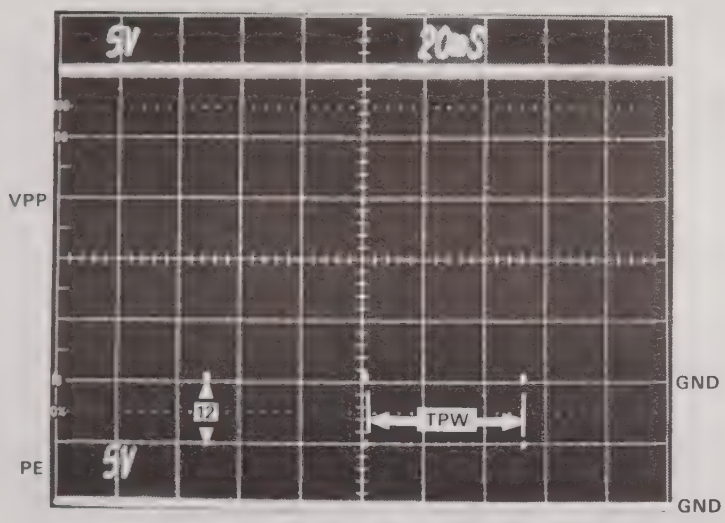
TIMING DIAGRAM

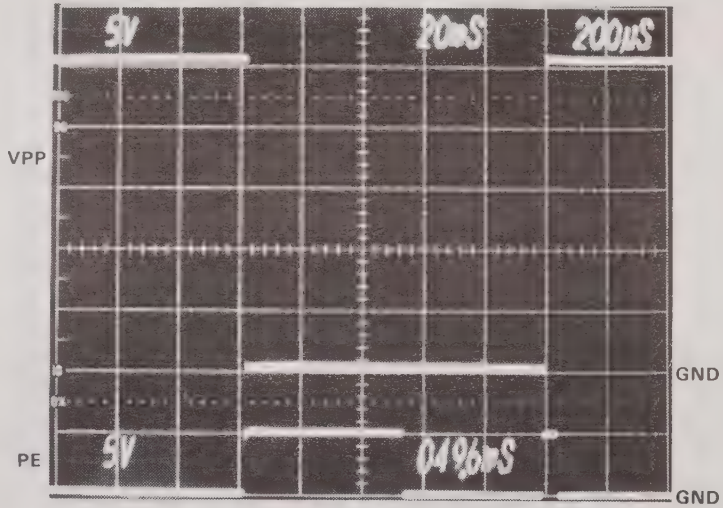
FAMILY CODES 19, 20

DATA I/O

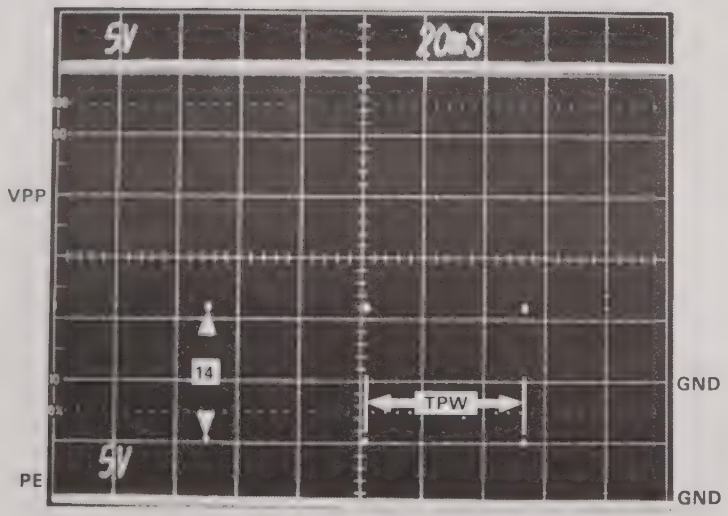
0526 128


5V
20mS
VPP
12
TPW
GND
PE
5V
GND

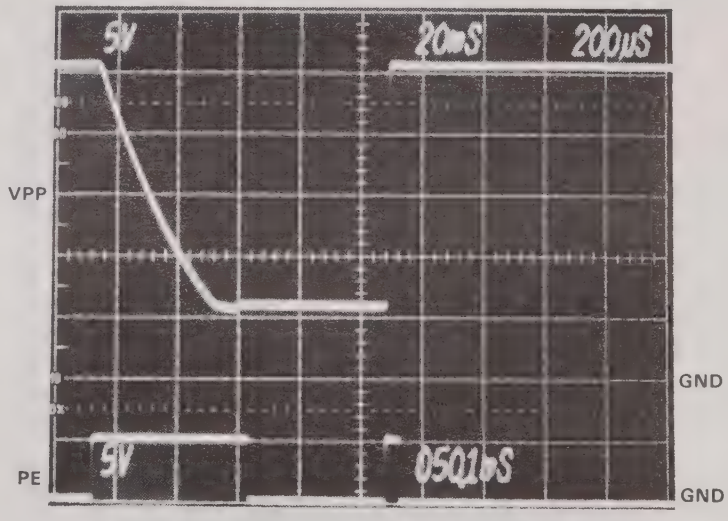
11


5V
20mS
200µS
VPP
GND
PE
5V
GND

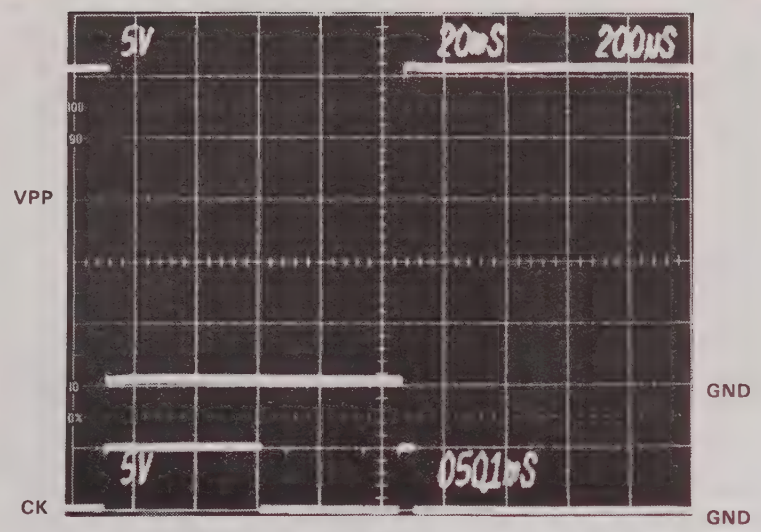
12


5V
20mS
VPP
14
TPW
GND
PE
5V
GND

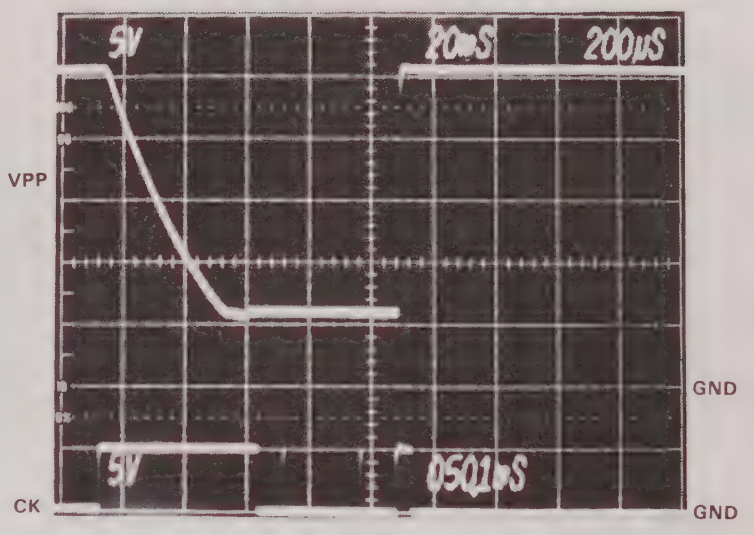
13


5V
20mS
200µS
VPP
GND
PE
5V
GND

14



15



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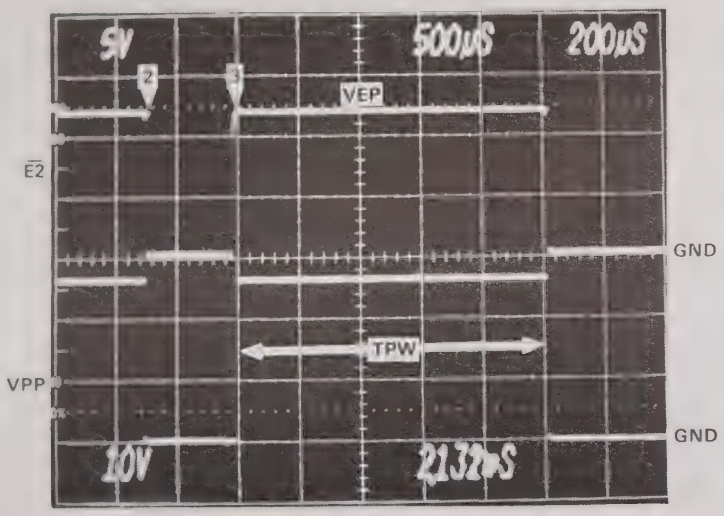
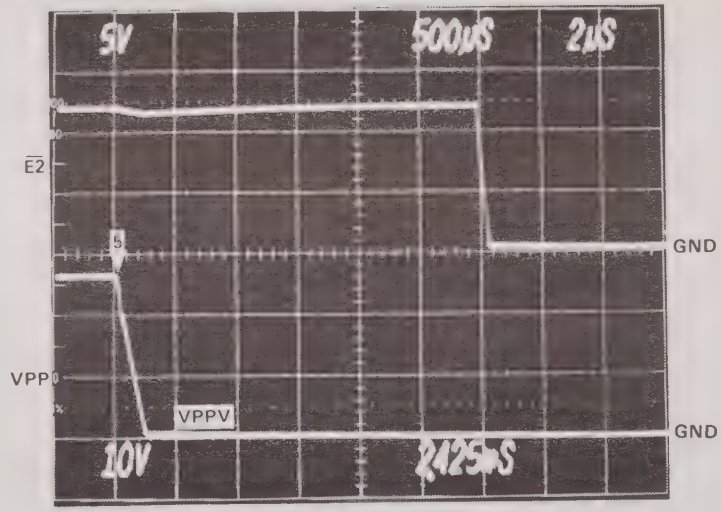
TIMING DIAGRAM

FAMILY CODES 19, 20

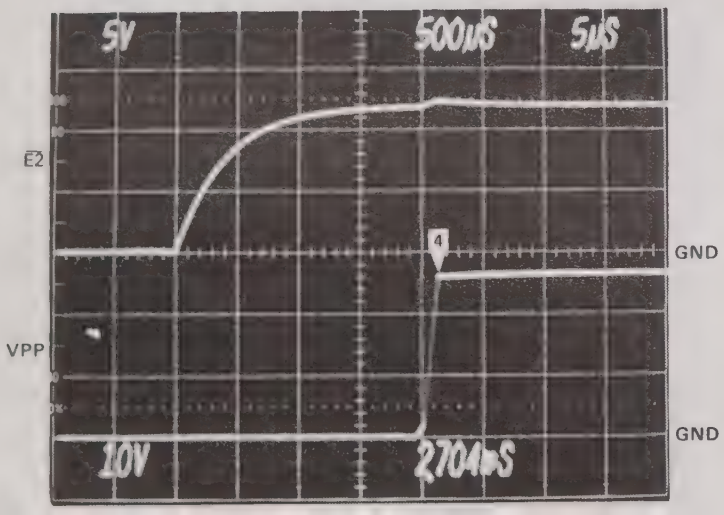
DATA I/O

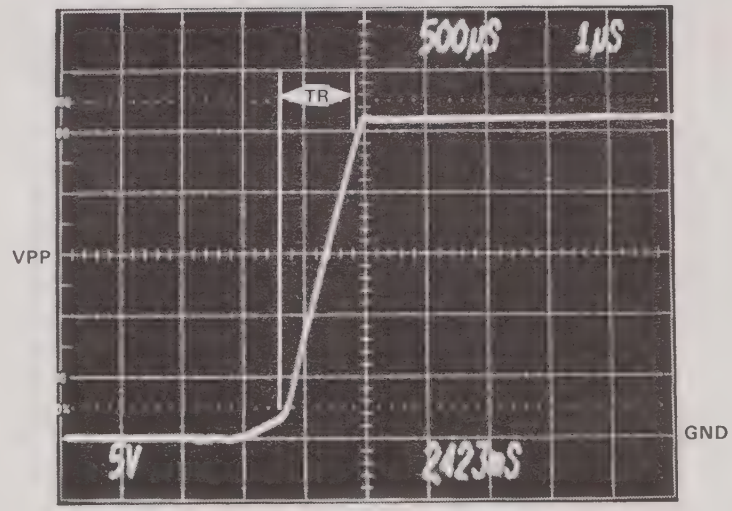

5V
500µS
200µS
VEP
E2
GND
TPW
VPP
GND
10V
2132µS

1


5V
500µS
2µS
E2
GND
VPP
VPPV
GND
10V
2125µS

2


5V
500µS
5µS
E2
GND
VPP
GND
10V
2704µS


500µS
1µS
TR
VPP
GND
5V
2423µS

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	25.0	26.0	27.0	V	
	VPPV	0.0	0.0	1.0	V	
	VEP	11.4	12.0	12.6	V	
	VBB	-5.25	-5.00	-4.75	V	Not Shown
	VDD	11.4	12.0	12.6	V	Not Shown
	TPW	0.8	1.0	1.2	ms	
	TR	0.5	1.0	2.0	µs	
	TF	0.5	1.0	2.0	µs	
	Reject		100		Loops	See Note 3
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	16.4	17.4	18.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 21.*
2. *Load RAM with hex 01 for Family 22, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *A loop is defined as a complete pas from Address 0 to maximum device address applying, one pulse at each address.*

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TIMING DIAGRAM

FAMILY CODES 21, 22

DATA I/O

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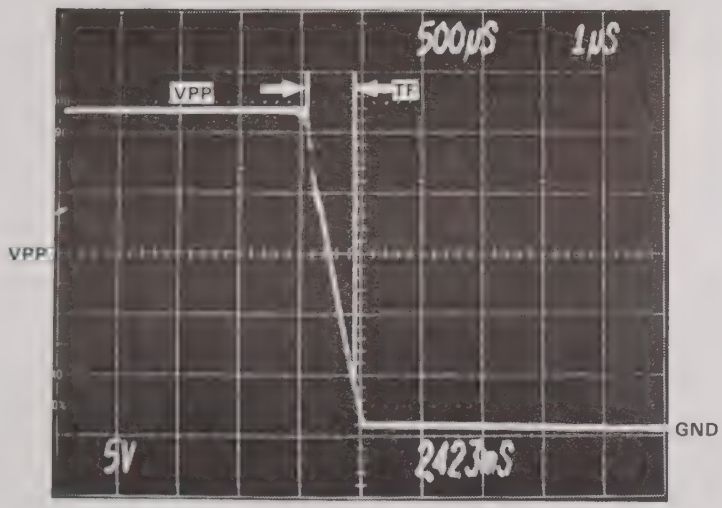
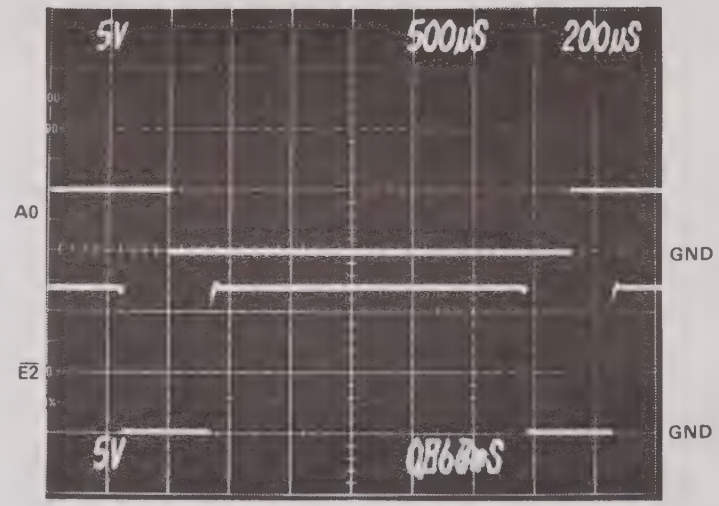
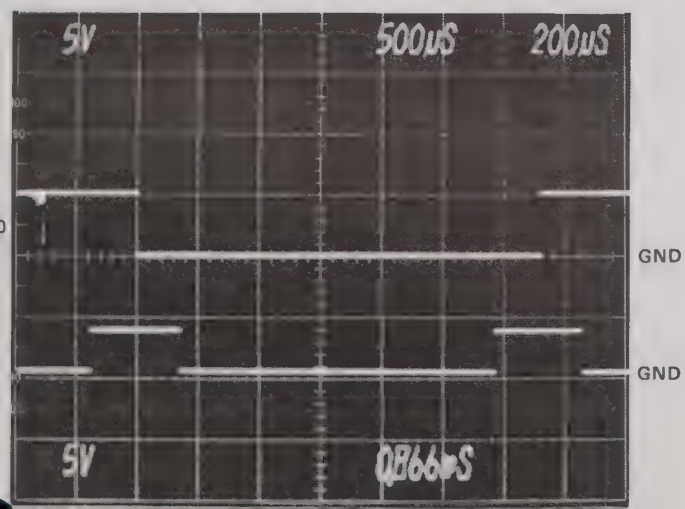
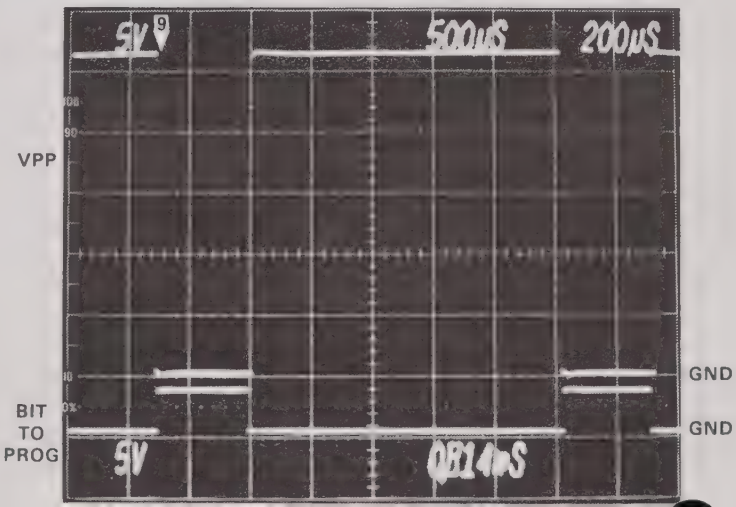

500µS
1µS
VPP
TF
VPP
GND
5V

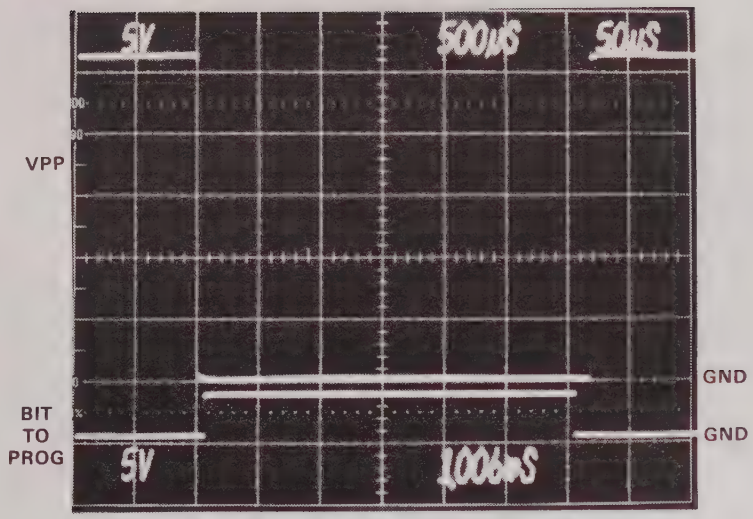
5


5V
500µS
200µS
A0
GND
E2
GND
5V

6


5V
500µS
200µS
A0
GND
BIT
TO
PROG
GND
5V


5V
500µS
200µS
VPP
GND
BIT
TO
PROG
GND
5V



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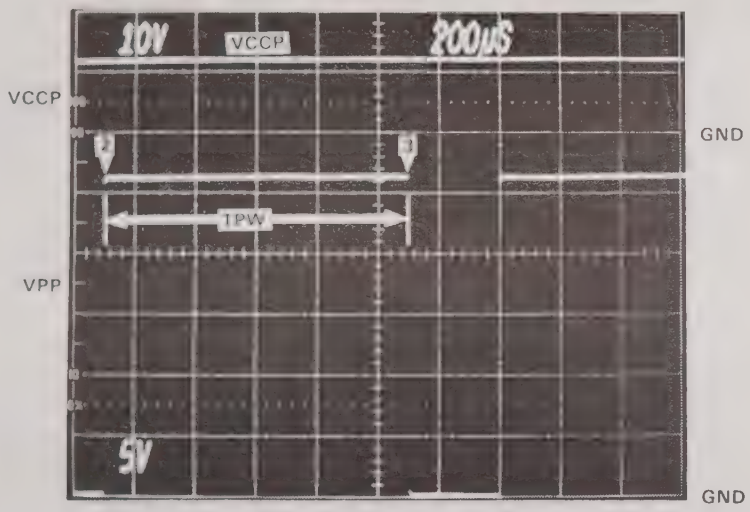
TIMING DIAGRAM

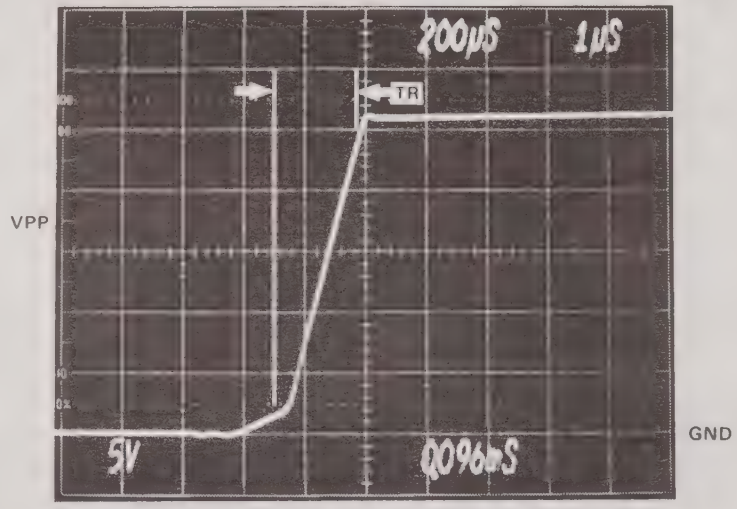
FAMILY CODES 21, 22

DATA I/O

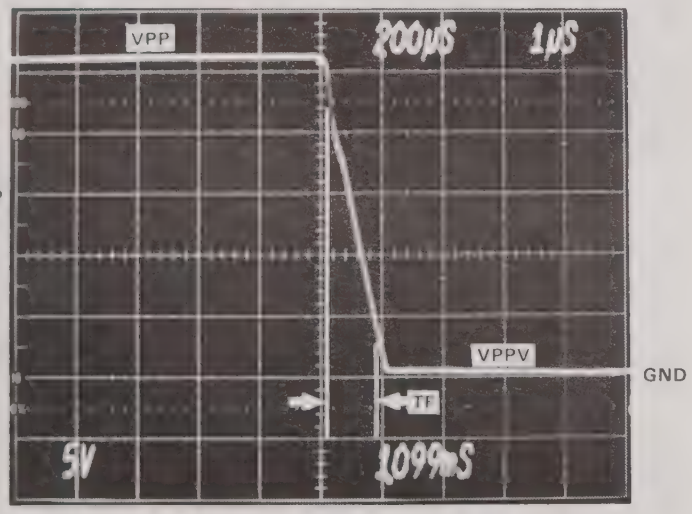
0526 1282


10V
VCCP
200µS
VCCP
GND
TPW
VPP
5V
GND

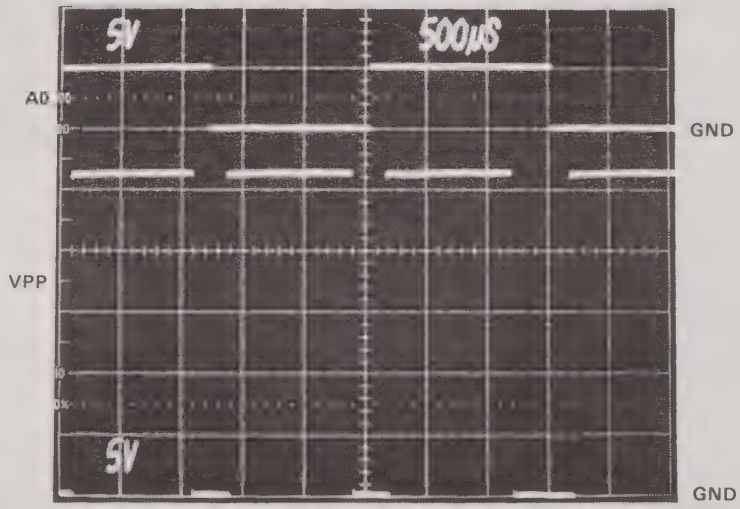
1


200µS
1µS
TR
VPP
5V
GND

2


VPP
200µS
1µS
VPP
VPPV
GND
TF
5V

3


5V
500µS
AD
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.4	12.0	12.6	V	
	VOP					NA
	VPP	25.0	26.0	27.0	V	
	VPPV	0.0		1.0	V	
	VBB	-5.25	-5.0	-4.75	V	Not Shown
	VDD	11.4	12.0	12.4	V	Not Shown
	TPW	0.8	1.0	1.2	ms	
	TR	0.5		2.0	µs	
	TF	0.5		2.0	µs	
	Reject		100		Loops	See Note 3
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	16.4	17.4	18.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 23.*
2. *Load RAM with hex 01 for Family 24, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *A loop is defined as a complete pass from Address 0 to maximum device address applying one pulse at each address. All 100 loops are performed, and the device is read and verified after all 100 loops.*

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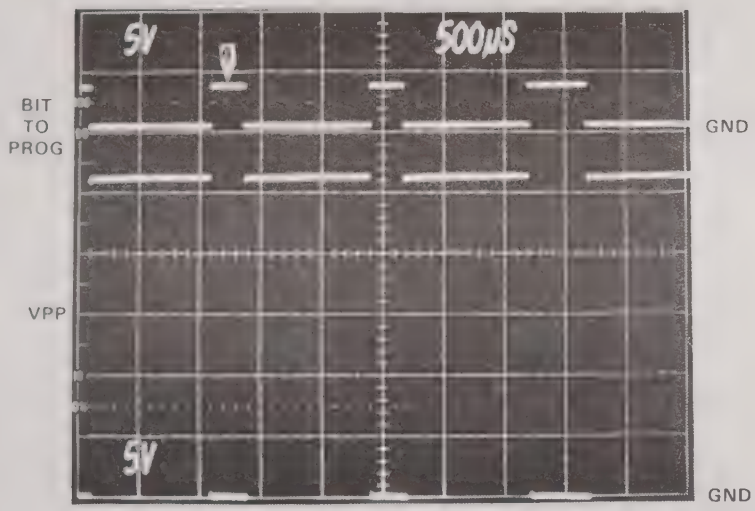
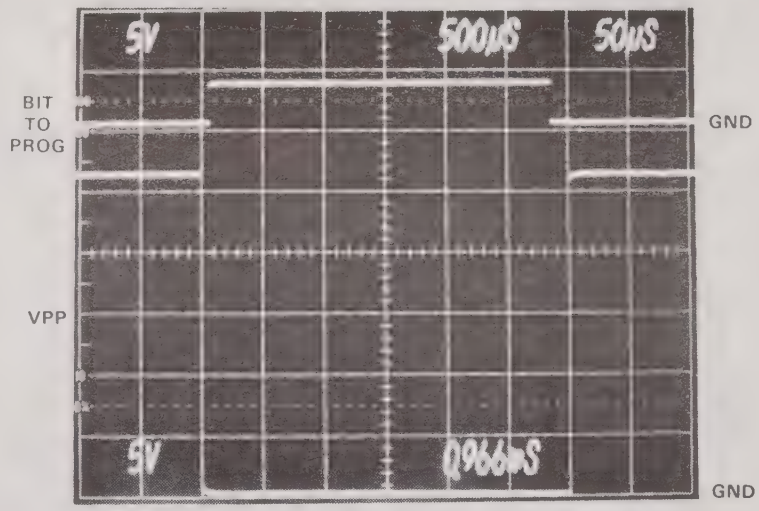
TIMING DIAGRAM

FAMILY CODES 23, 24

DATA I/O


5V
500µS
BIT
TO
PROG
GND
VPP
5V
GND

5


5V
500µS
50µS
BIT
TO
PROG
GND
VPP
5V
GND

6

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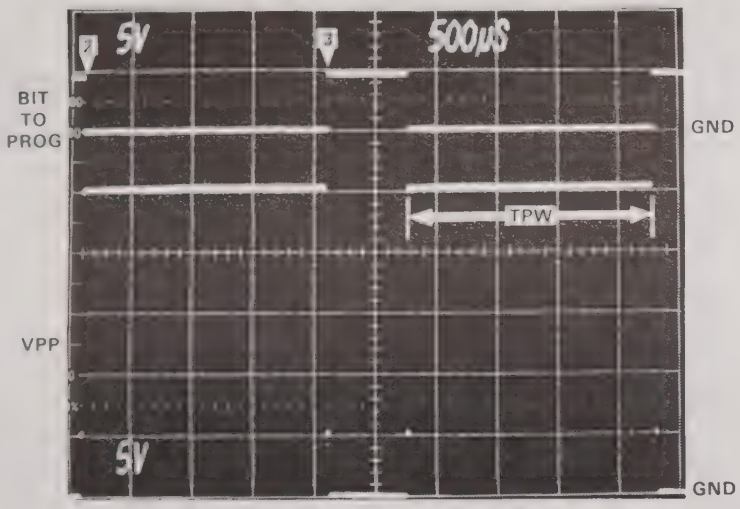
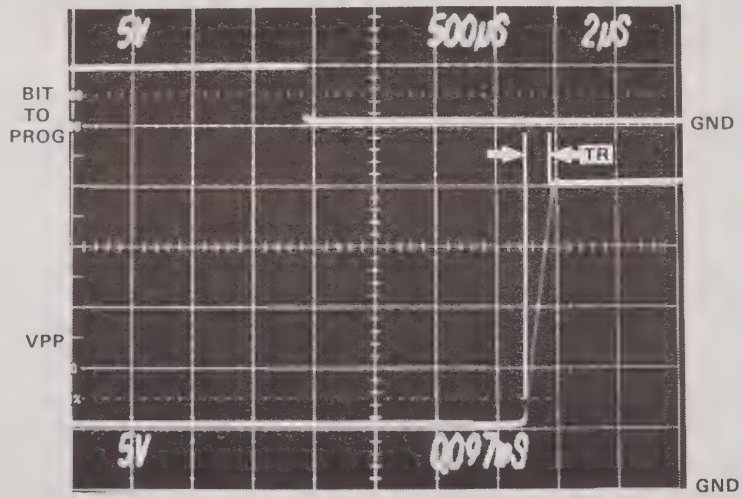
TIMING DIAGRAM

FAMILY CODES 23, 24

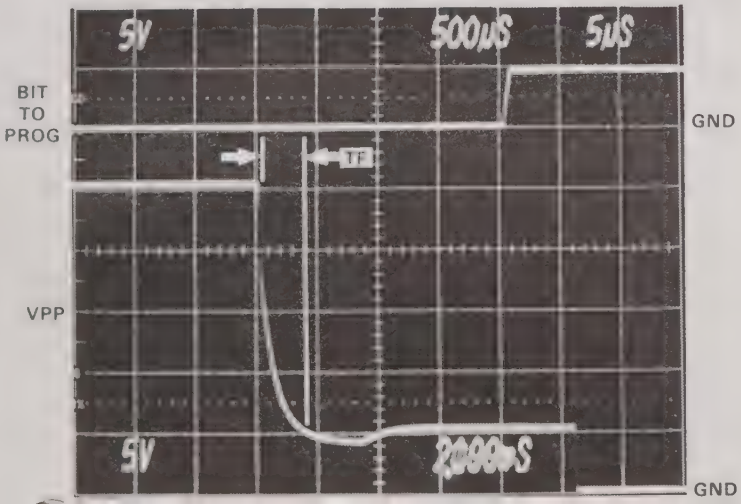
DATA I/O

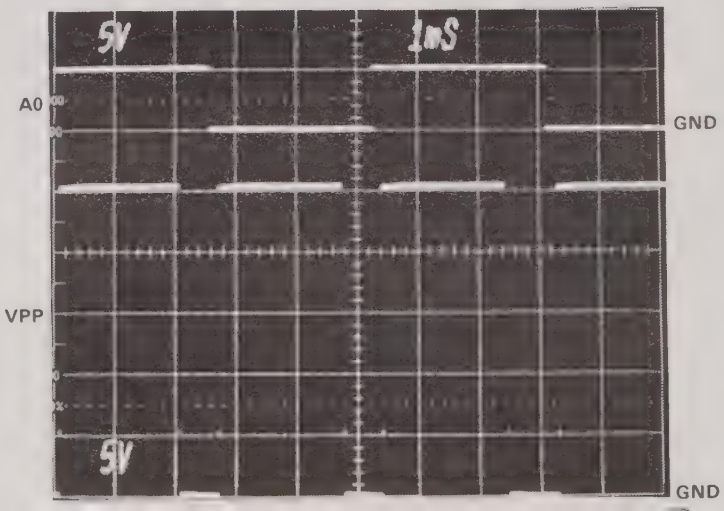

5V
500µS
BIT
TO
PROG
GND
TPW
VPP
5V
GND

1


5V
500µS
2µS
BIT
TO
PROG
GND
TR
VPP
5V
GND

2


5V
500µS
5µS
BIT
TO
PROG
GND
TF
VPP
5V
GND


5V
1mS
A0
GND
VPP
5V
GND

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	1.9	2.0	2.1	ms	
	TR	0.5		2.0	µs	
	TF	0.5		5.0	µs	
	Reject		20		Loops	See Note 3
	Overprogram		5		Loops	See Note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Looad RAM with hex FE for Family 25.*
2. *Load RAM with hex 01 for Family 26, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *A loop is defined as one complete pass from Address 0 to maximum device address applying one pulse at each address. A read and verify is done after each loop, and when the device verifies, five more loops are applied.*

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TIMING DIAGRAM

FAMILY CODES 25, 26

DATA I/O

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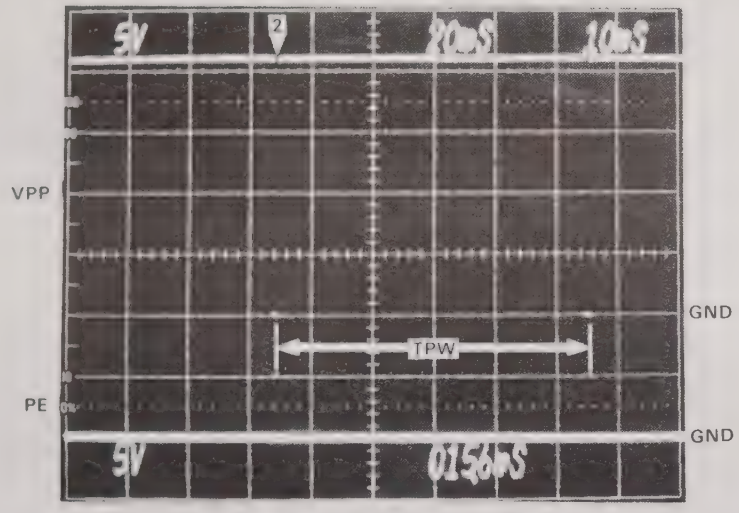
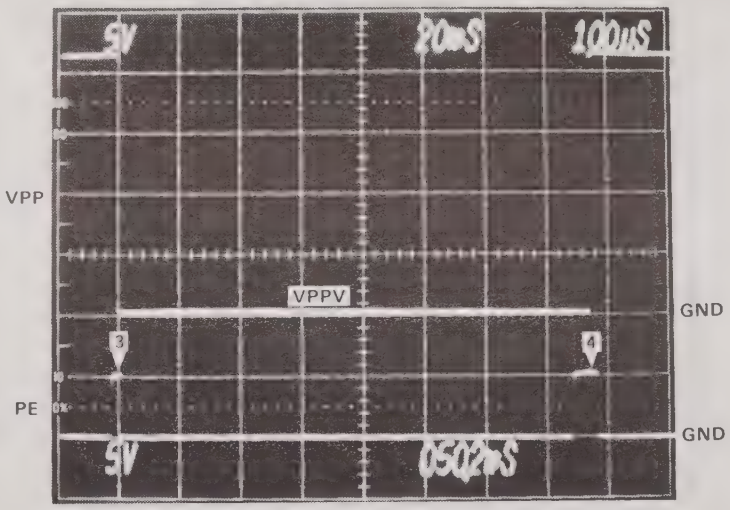
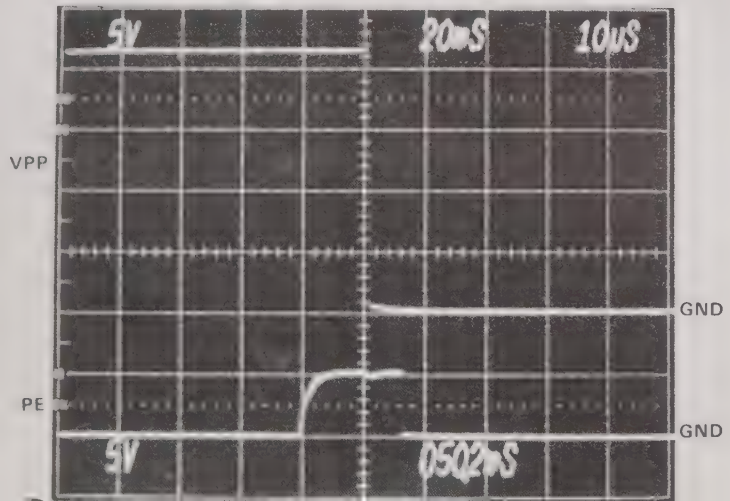
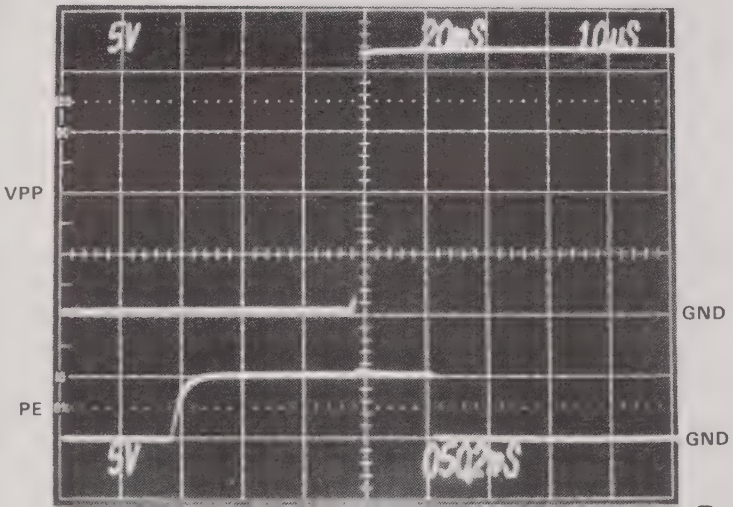

5V
2
20mS
10mS
VPP
GND
TPW
PE
GND
5V
0156mS

1


5V
20mS
100uS
VPP
VPPV
GND
3
4
PE
GND
5V
0502mS

2


5V
20mS
10uS
VPP
GND
PE
GND
5V
0502mS


5V
20mS
10uS
VPP
GND
PE
GND
5V
0502mS

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.00	6.00	V	
	VPP	20.5	21.0	21.5	V	
	VPPV	0.0	0.0	0.8	V	
	TPW	48	50	52	ms	
	TR	50			ns	
	TF					NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 27.*
2. *Load RAM with hex 01 for Family 28, and bit-to-prog waveform becomes bit-no-prog waveform.*

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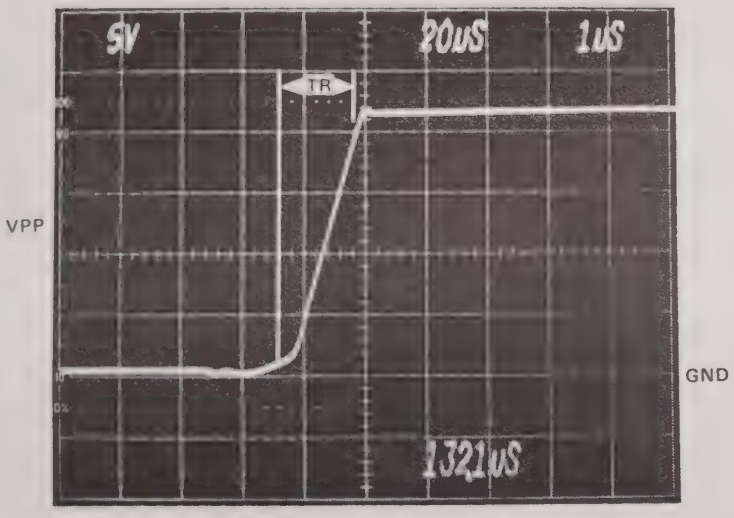
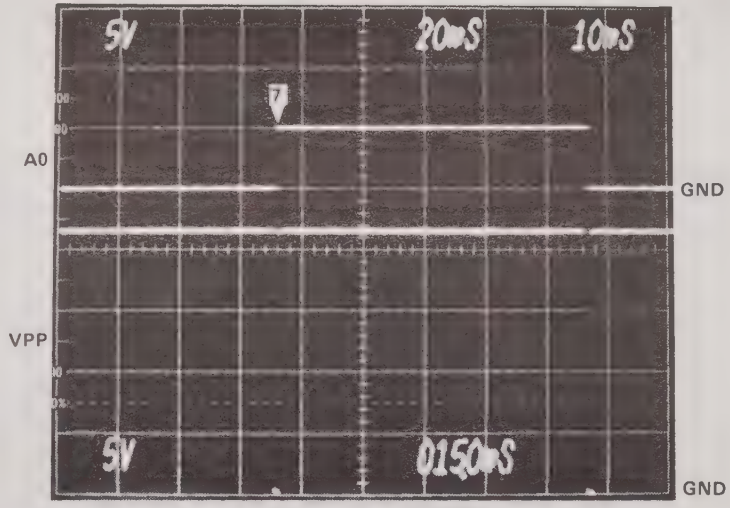
TIMING DIAGRAM

FAMILY CODES 27, 28

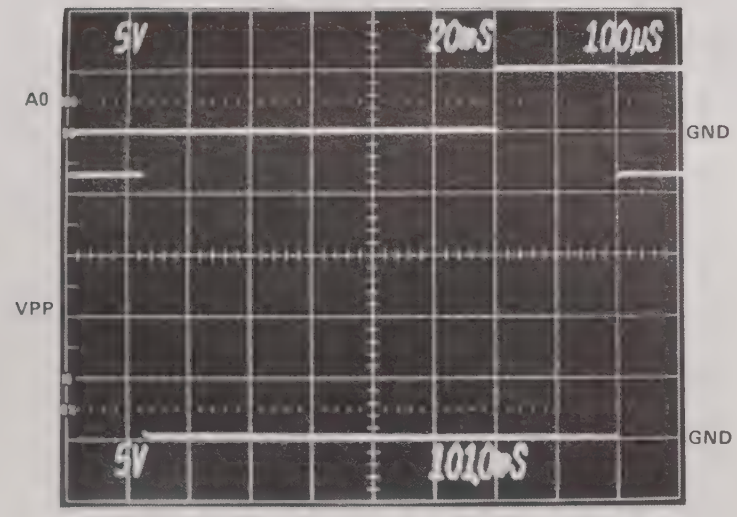
DATA I/O

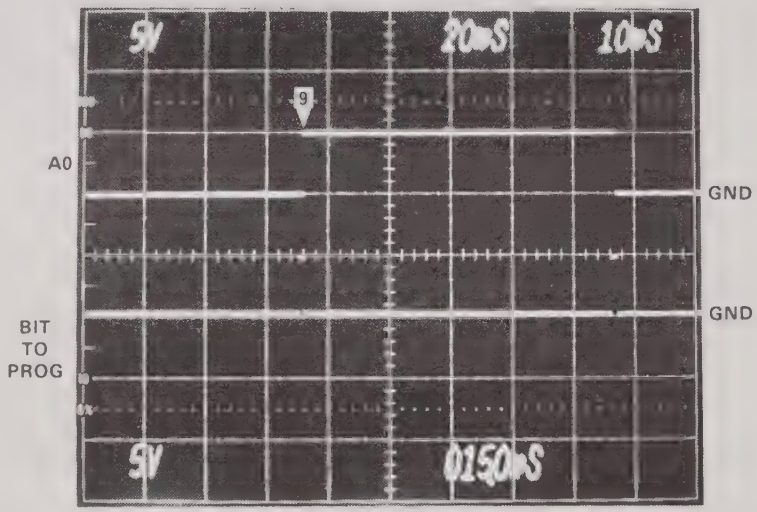

5V
20µS
1µS
TR
VPP
GND
1321µS

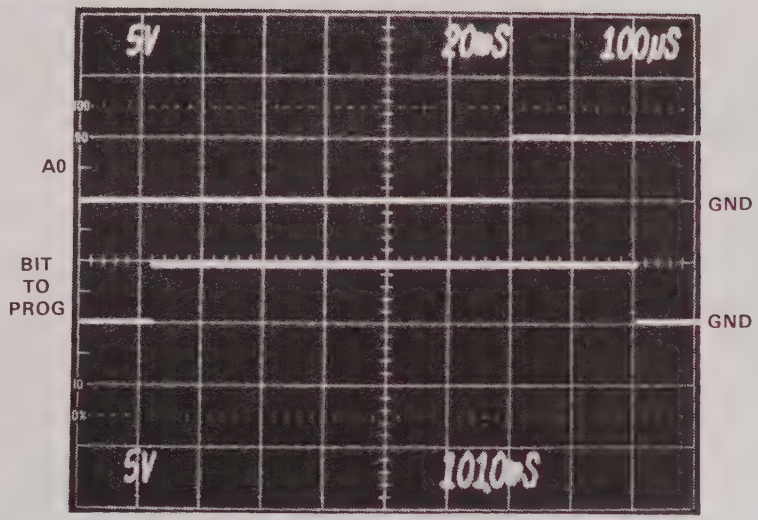
5


5V
20mS
10mS
7
A0
GND
VPP
5V
0150mS
GND

6


5V
20mS
100µS
A0
GND
VPP
GND
5V
1010mS


5V
20mS
10mS
9
A0
GND
GND
BIT
TO
PROG
5V
0150mS



9

REVISIONS

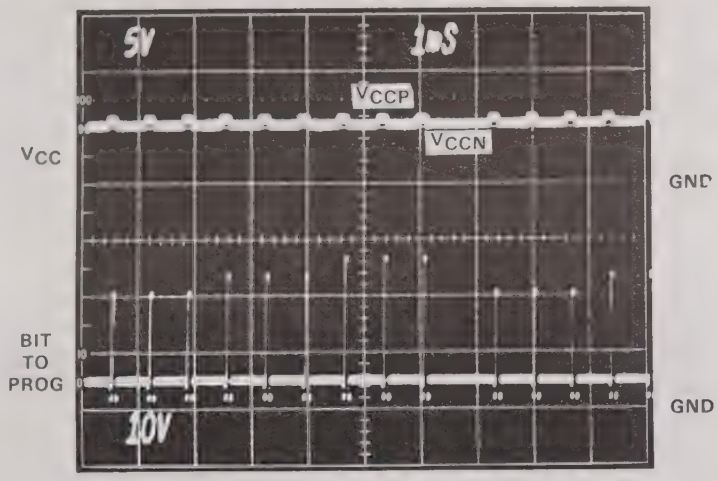
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

Sheet 2 of 2

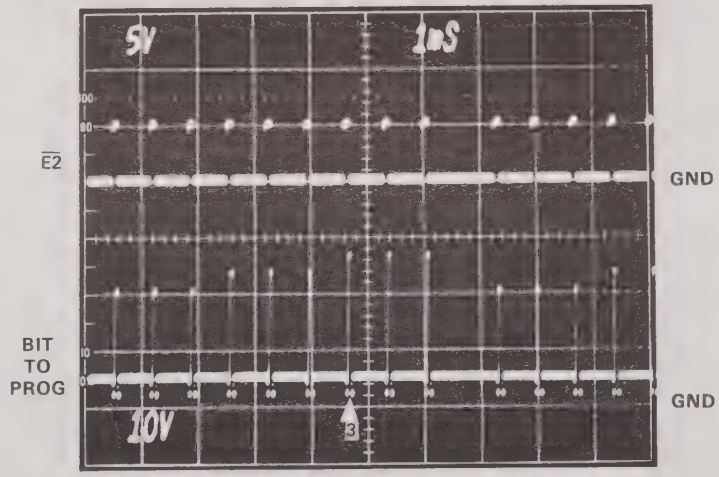
TIMING DIAGRAM

FAMILY CODES 27, 28

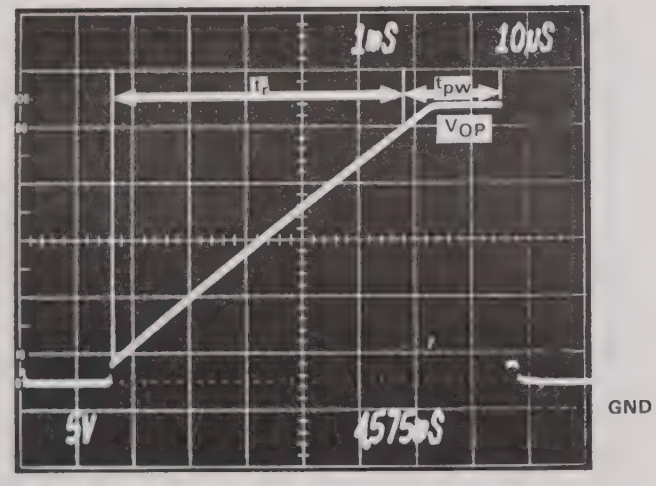
DATA I/O


5V
1mS
VCCP
VCCN
VCC
GND
BIT
TO
PROG
GND
10V

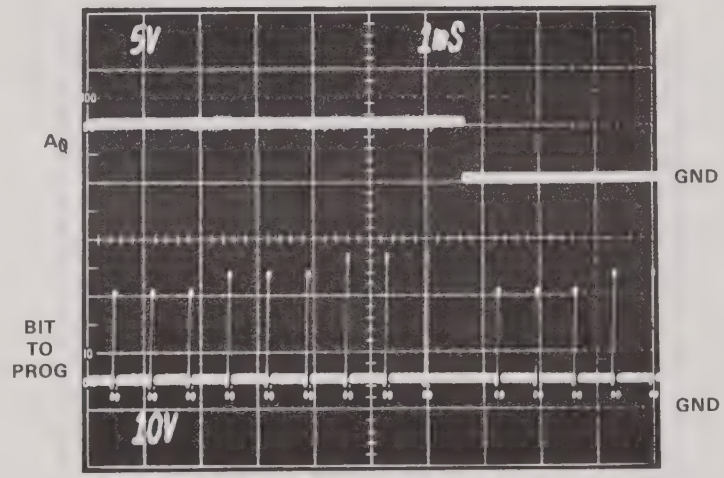
1


5V
1mS
E2
GND
BIT
TO
PROG
GND
10V
3

2


1mS
10µS
tr
tpw
VOP
BIT
TO
PROG
GND
5V
4575µS

3


5V
1mS
A0
GND
BIT
TO
PROG
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.4	5.5	5.6	V	
	V_{CCN}	4.75	5.0	5.25	V	
	V_{OP}	19	20	21	V	Pulse 1-3
		22	23	24	V	Pulse 4-6
		25	26	27	V	Pulse 7-9
	t_{pw}	10		40	us	See Note 3
	t_r	42	52	69	us	See Note 4
	Reject		9		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.1	4.2	4.3	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	17.3	18.3	19.3	V	701-1998/TP3
	LOW LOAD	17.3	18.3	19.3	V	701-1998/TP2
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	2.9	3.0	3.1	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP3
	LOW LOAD	5.2	5.7	6.2	V	701-1998/TP2

NOTES

1. *Load RAM with hex FE for Family 29*
2. *Load RAM with hex 01 for Family 30.*
3. *This is measured at the 90% level of the pulse, and all three pulse levels must meet this specification.*
4. *This is measured from 10% to 90% on the 26V pulse.*

REVISIONS

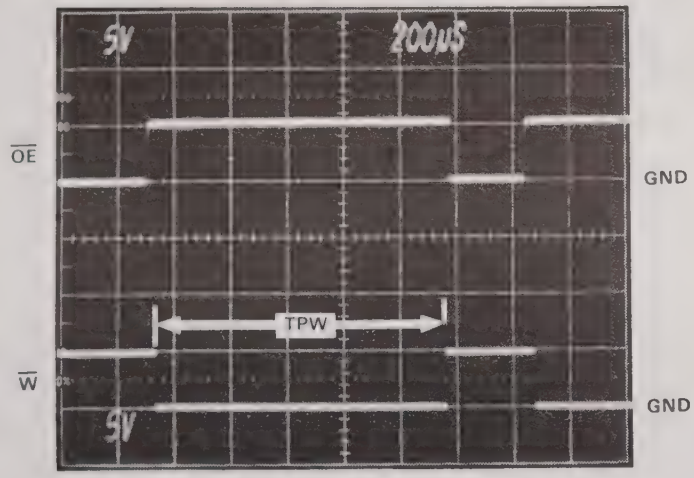
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CJZ	3/84

Sheet 1 of 1

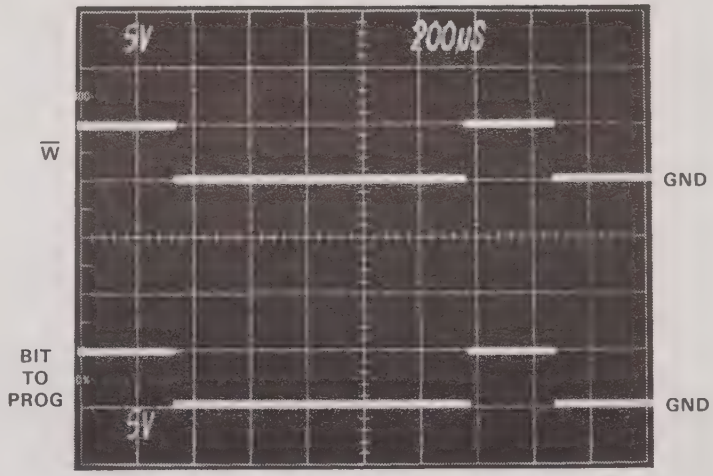
TIMING DIAGRAM

FAMILY CODES 29, 30

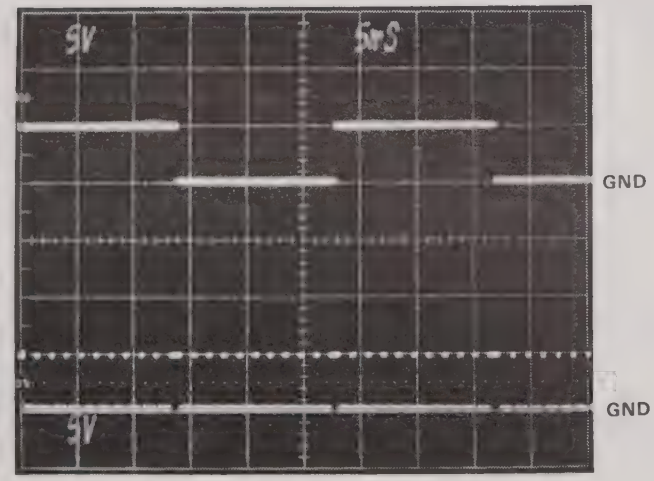
DATA I/O


5V
200uS
OE
GND
TPW
W
GND
5V

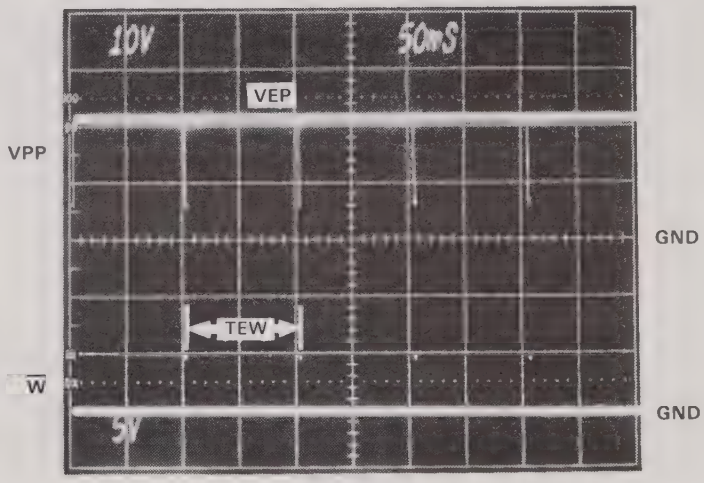
1


5V
200uS
W
GND
BIT
TO
PROG
GND
5V

2


5V
5mS
A0
GND
BIT
TO
PROG
GND
5V

3


10V
50mS
VEP
VPP
GND
TEW
W
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VEP	19.5	20.0	20.5	V	
	VEE	19.5	20.0	20.5	V	
	TPW	1.0		10.0	ms	
	TEW	99	100	101	ms	
	Reject		10		Pulse	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.0	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	3.9	4.9	5.9	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 2D.*
2. *Load RAM with hex 01 for Family 2E.*
3. *Photos 4 and 5 show erase pulse.*

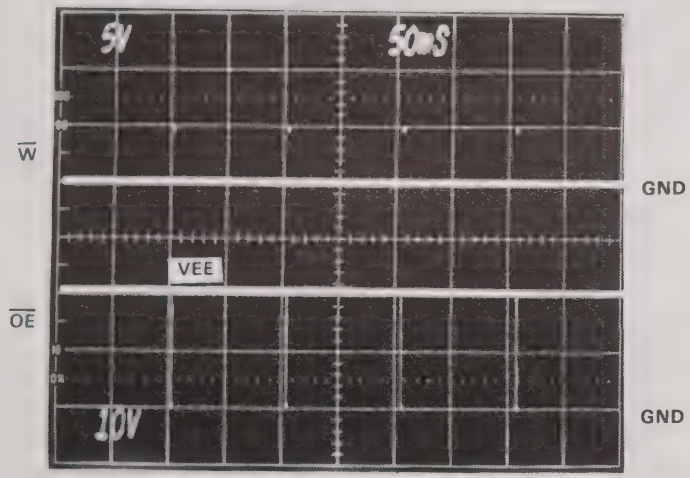
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

TIMING DIAGRAM

FAMILY CODES 2D, 2E

DATA I/O



5

REVISIONS

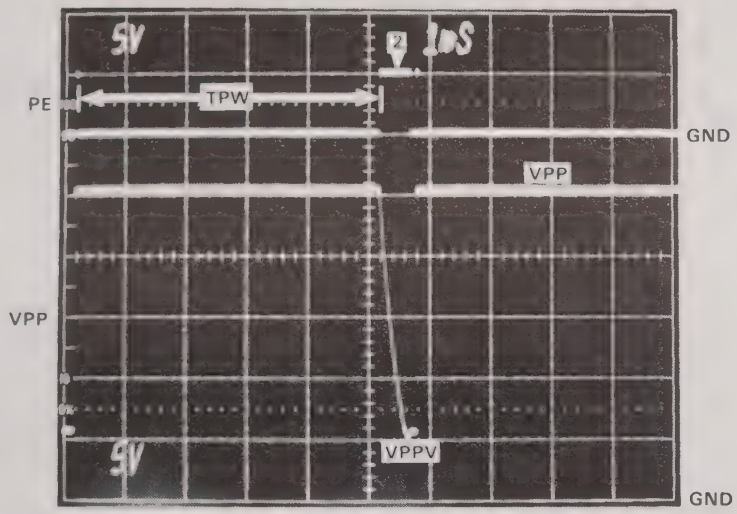
LTR	DESCRIPTION	P.E.	DATE

Sheet 2 of 2

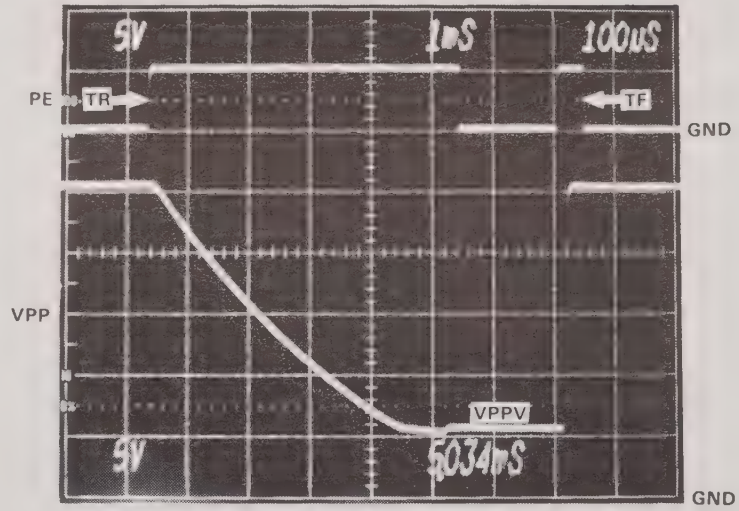
TIMING DIAGRAM

FAMILY CODES 2D, 2E

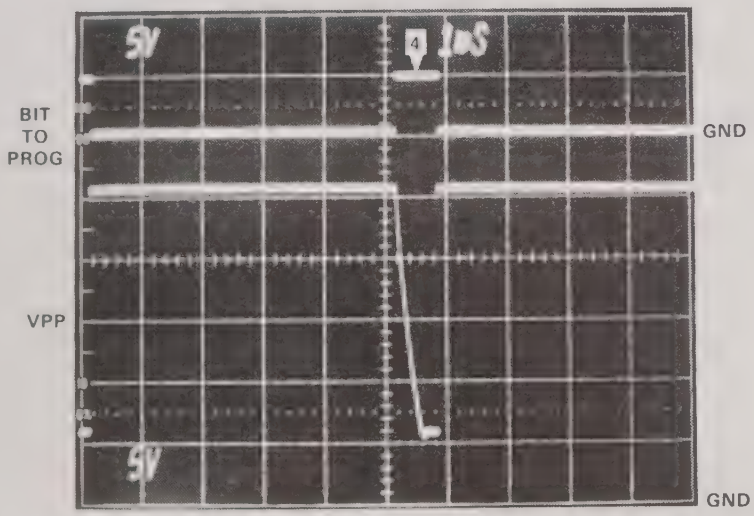
DATA I/O


5V
1mS
PE
TPW
GND
VPP
VPP
VPPV
5V
GND

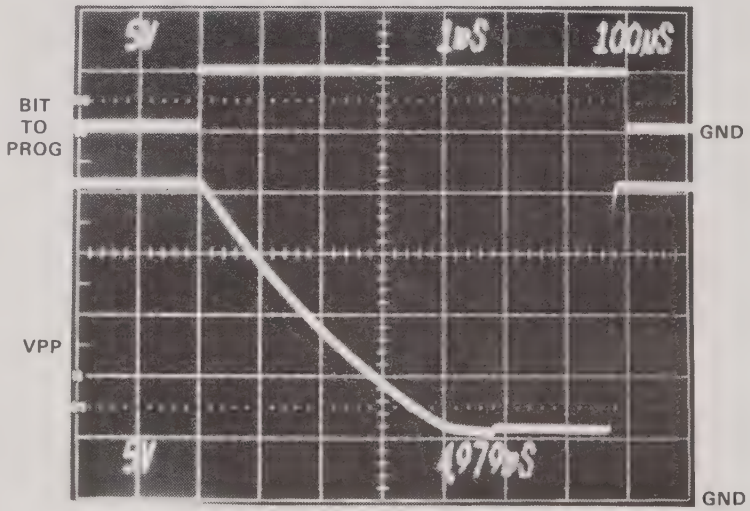
1


5V
1mS
100uS
PE
TR
TF
GND
VPP
VPPV
5V
GND

2


5V
1mS
BIT
TO
PROG
GND
VPP
5V
GND

3


5V
1mS
100uS
BIT
TO
PROG
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	4.9	5.0	5.1	ms	
	TR	5			ns	
	TF	5			ns	
	Reject		5		Pulses	
	Overprogram		x		Pulses	See Note 3
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 31.*
2. *Load RAM with hex 01 for Family 32, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The number of overprogram pulses is equal to the greatest number of reject pulses applied to any address.*

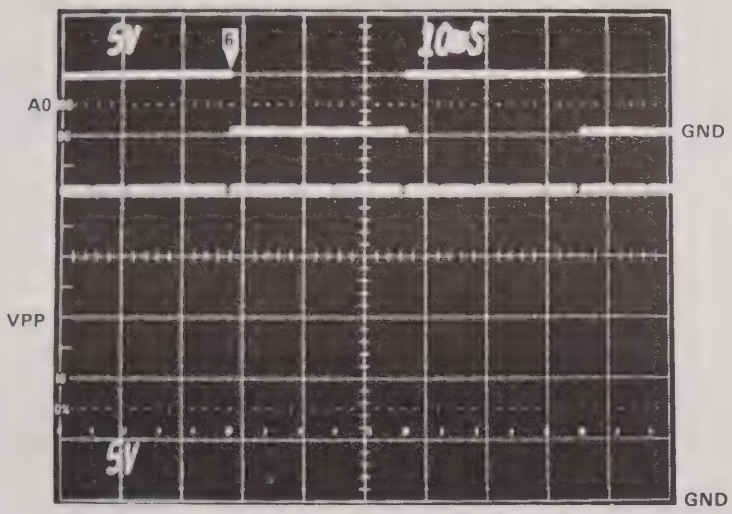
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTS	3/84

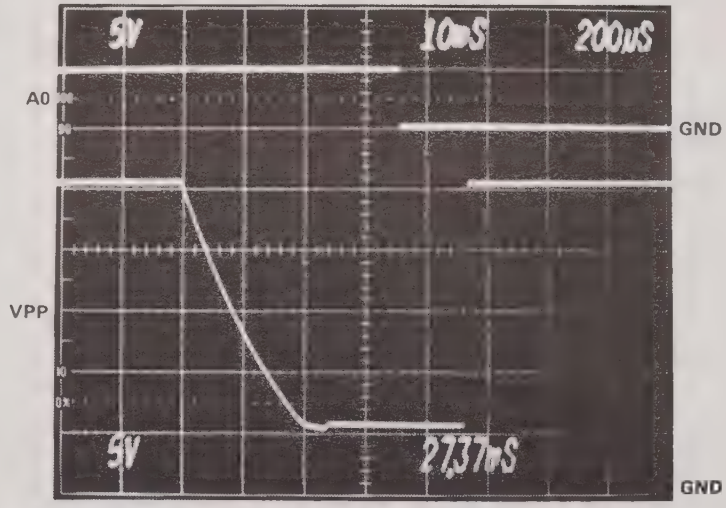
TIMING DIAGRAM

FAMILY CODES 31, 32

DATA I/O



5



6

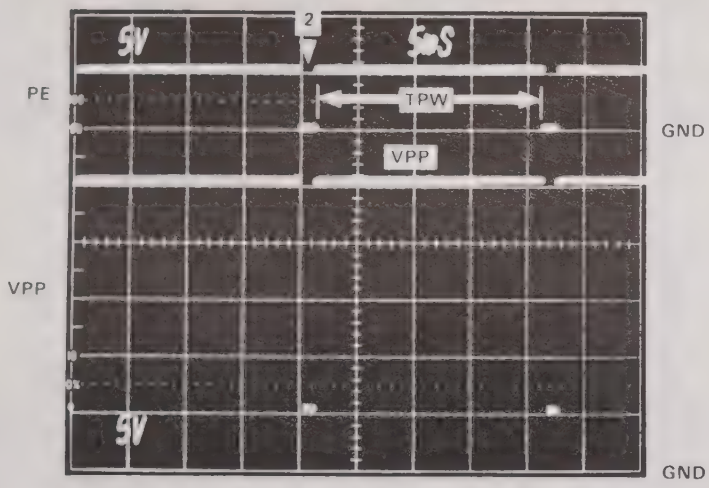
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

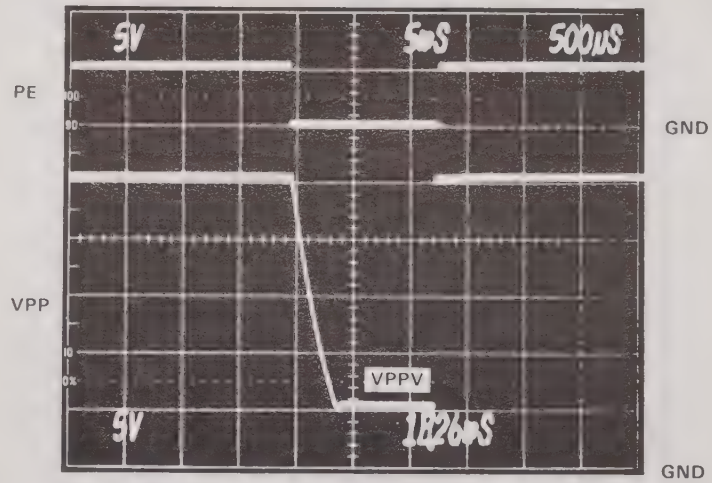
TIMING DIAGRAM

FAMILY CODES 31, 32

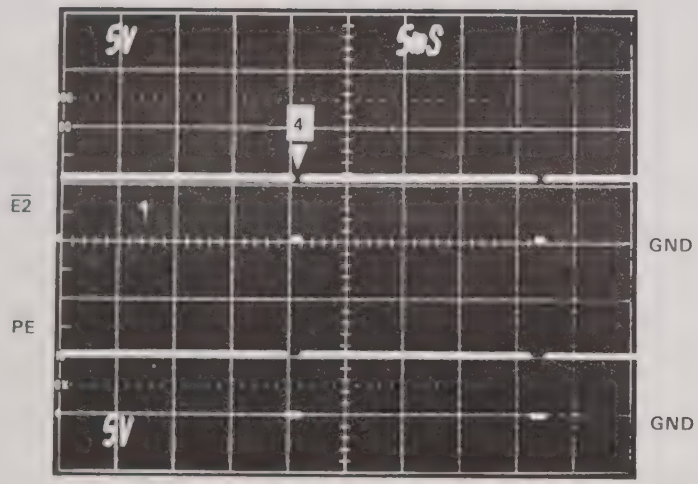
DATA I/O


5V
2
5mS
PE
TPW
GND
VPP
VPP
5V
GND

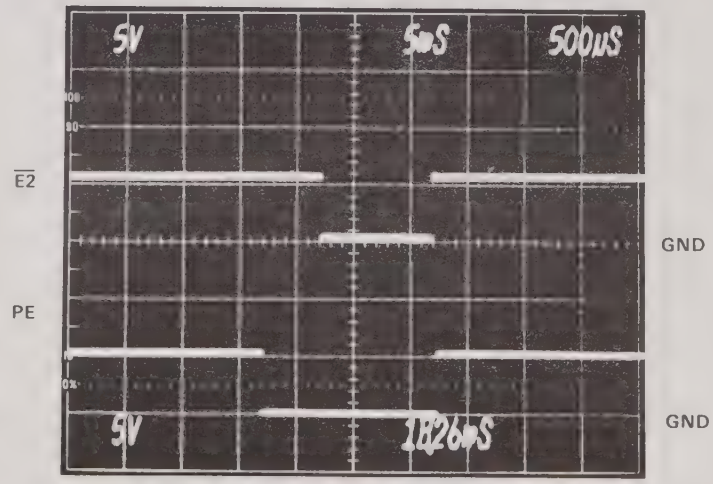
1


5V
5mS
500µS
PE
GND
VPP
VPPV
5V
1.826mS
GND

2


5V
5mS
4
E2
1
GND
PE
5V
GND

3


5V
5mS
500µS
E2
GND
PE
5V
1.826mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	19.8	20.0	20.2	ms	
	TR					NA
	TEW	200			ms	
	TF					NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 33.*
2. *Load RAM with hex 01 for Family 34, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photo 9 is the erase waveform.*

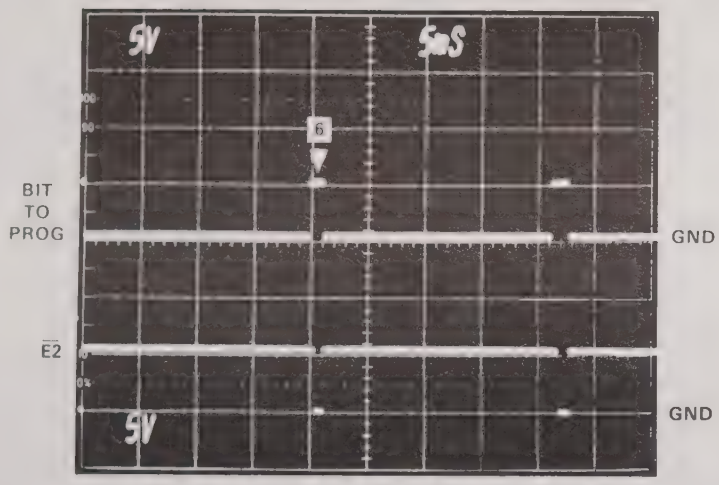
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

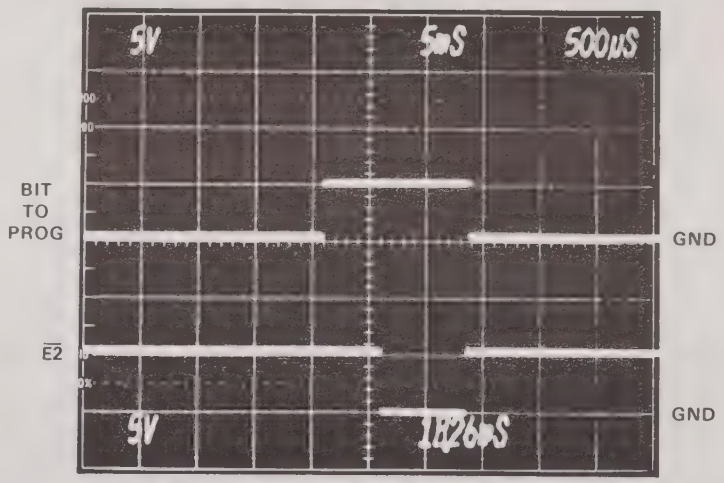
TIMING DIAGRAM

FAMILY CODES 33, 34

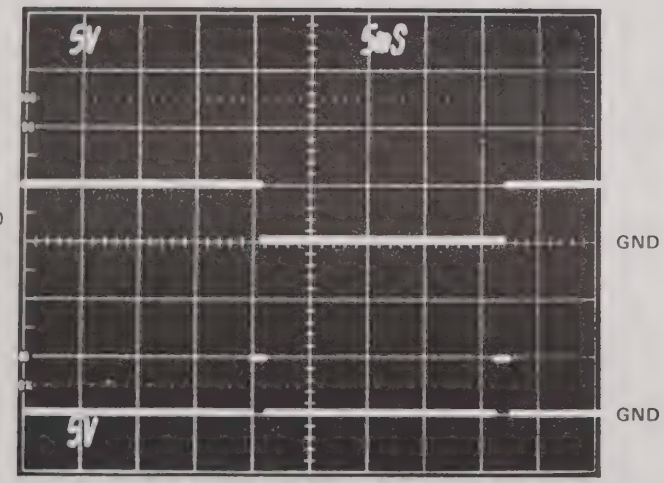
DATA I/O


5V
5mS
6
BIT
TO
PROG
GND
E2
GND
5V

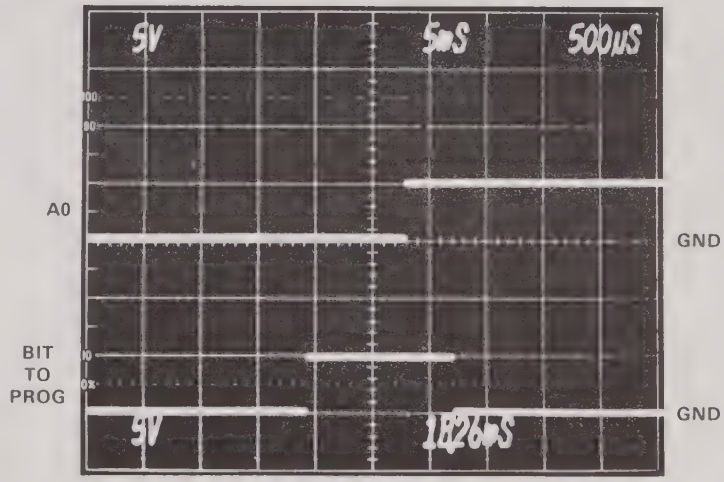
5


5V
5mS
500µS
BIT
TO
PROG
GND
E2
GND
5V
1.826mS

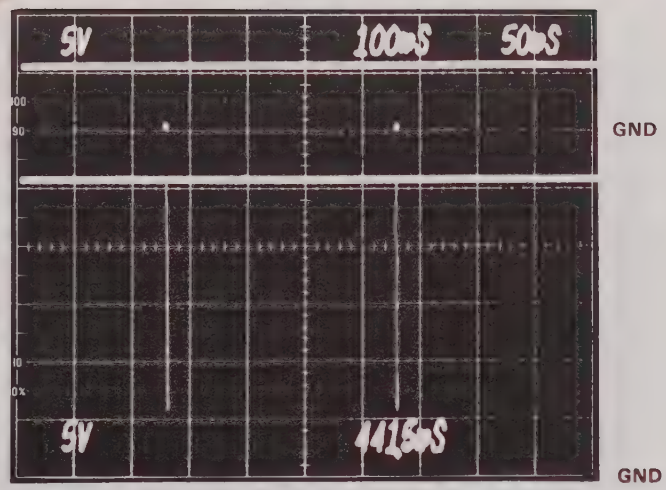
6


5V
5mS
A0
GND
BIT
TO
PROG
GND
5V

7


5V
5mS
500µS
A0
GND
BIT
TO
PROG
GND
5V
1.826mS

8



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981-0003

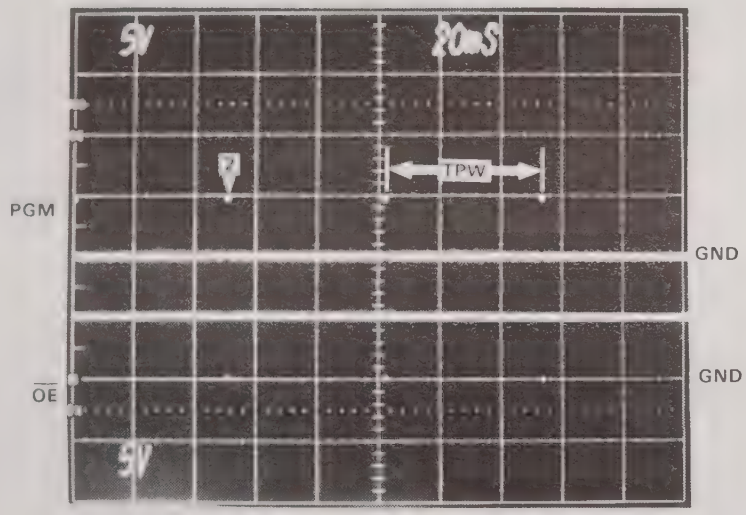
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

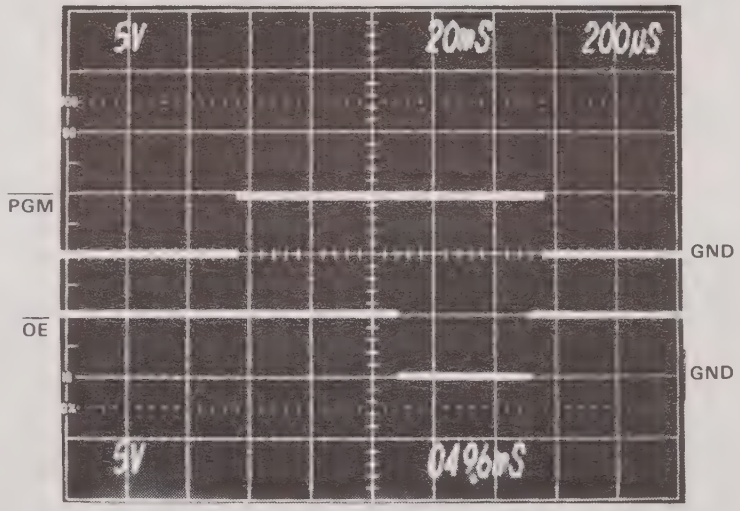
TIMING DIAGRAM

FAMILY CODES 33, 34

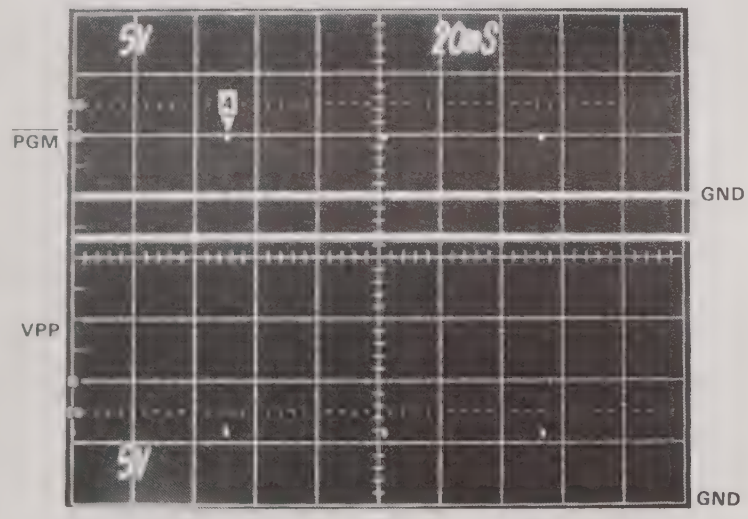
DATA I/O


5V
20mS
TPW
PGM
GND
OE
GND
5V

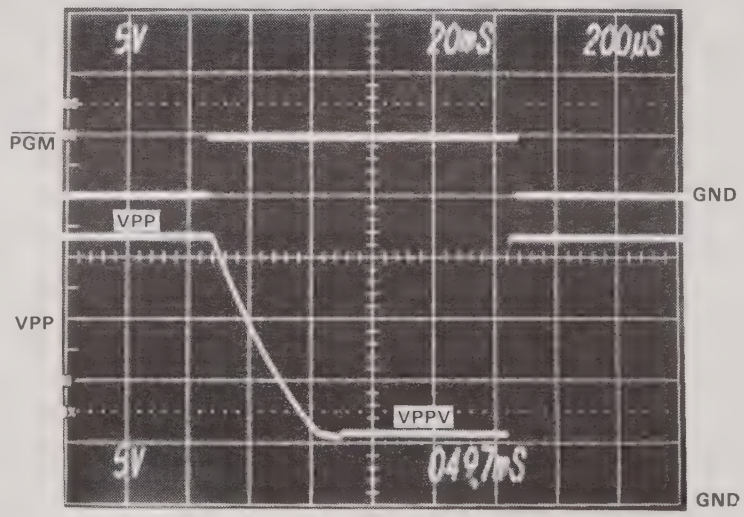
1


5V
20mS
200uS
PGM
GND
OE
GND
5V
0.96mS

2


5V
20mS
PGM
GND
VPP
5V
GND

3


5V
20mS
200uS
PGM
GND
VPP
VPP
VPPV
5V
0.97mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.00	5.25	V	
	TPW	48	50	52	ms	
	TR					NA
	TF					NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 35.*
2. *Load RAM with hex 01 for Family 36, and bit-to-prog waveform becomes bit-no-prog waveform.*

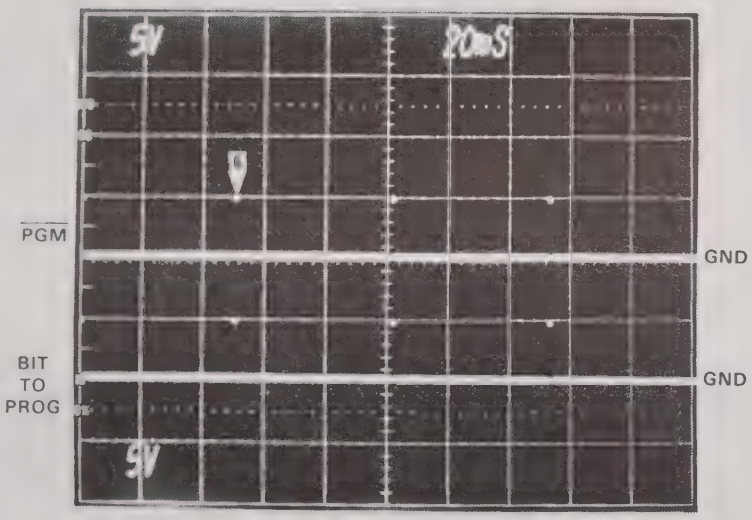
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

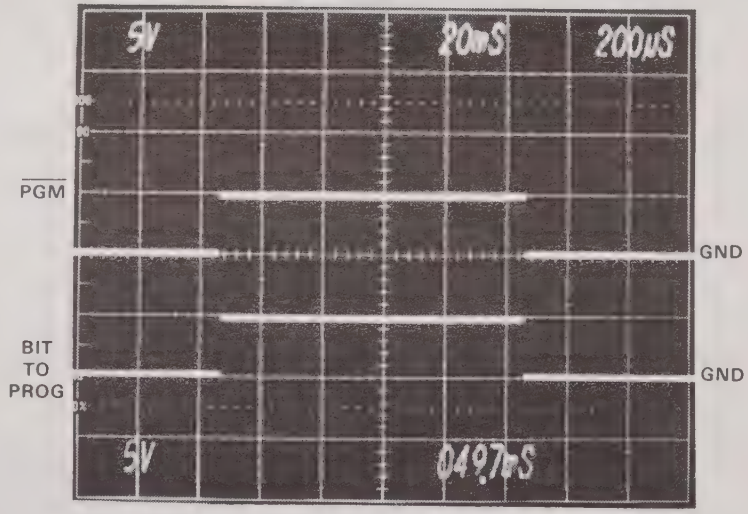
TIMING DIAGRAM

FAMILY CODES 35, 36

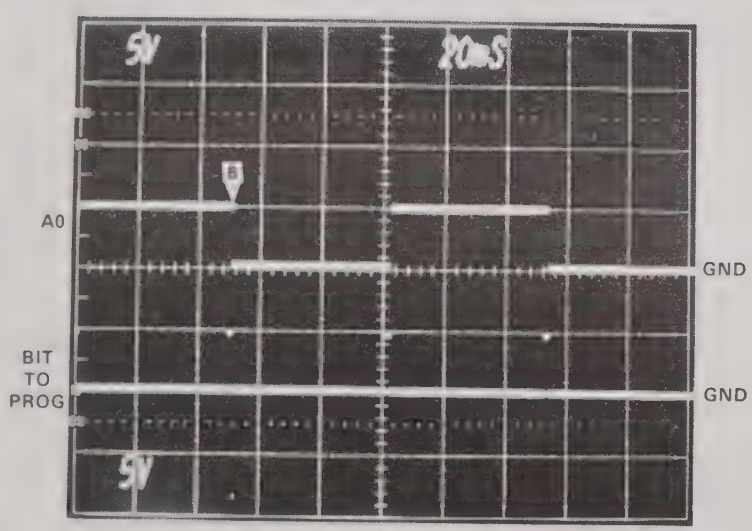
DATA I/O


5V
20mS
PGM
GND
BIT
TO
PROG
GND
5V

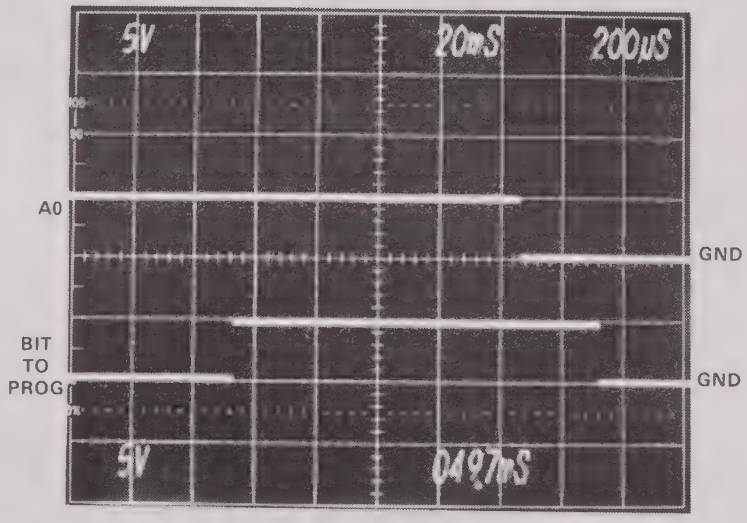
5


5V
20mS
200µS
PGM
GND
BIT
TO
PROG
GND
5V
049.7mS

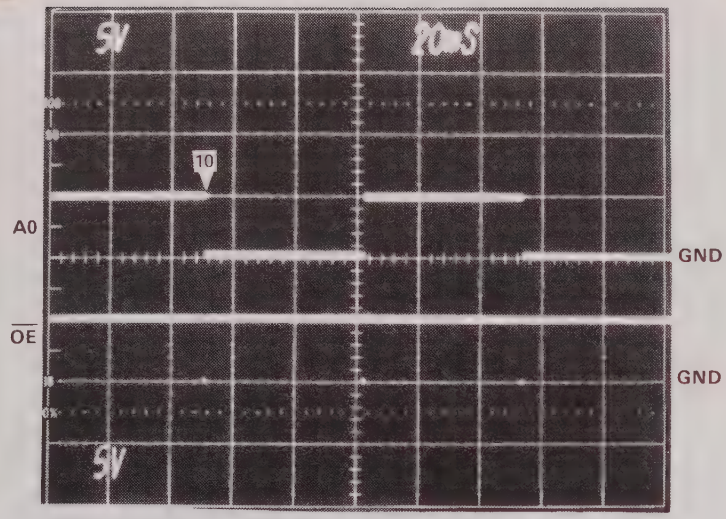
6


5V
20mS
A0
GND
BIT
TO
PROG
GND
5V

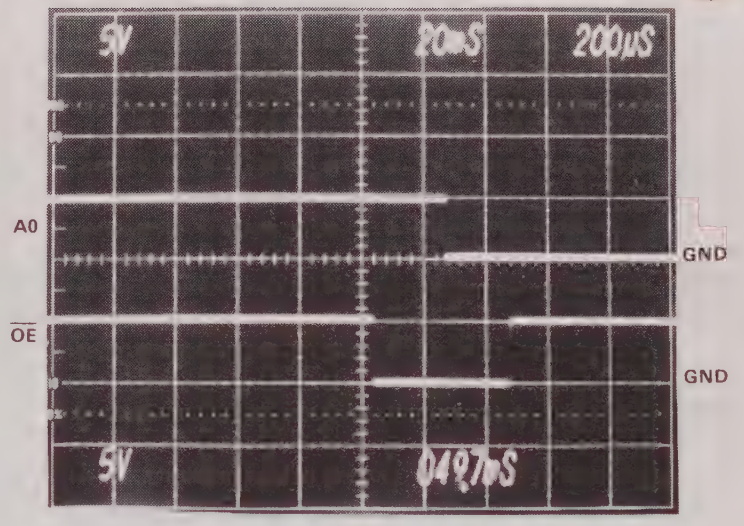
7


5V
20mS
200µS
A0
GND
BIT
TO
PROG
GND
5V
049.7mS

8



9



10

REVISIONS

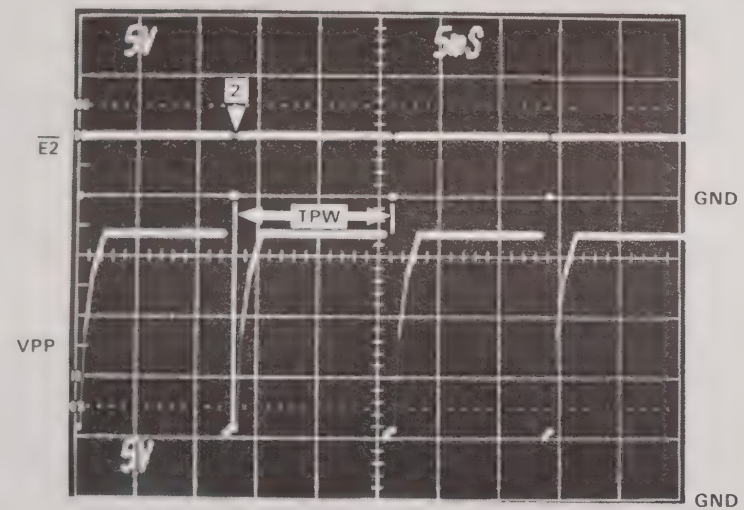
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

Sheet 2 of 2

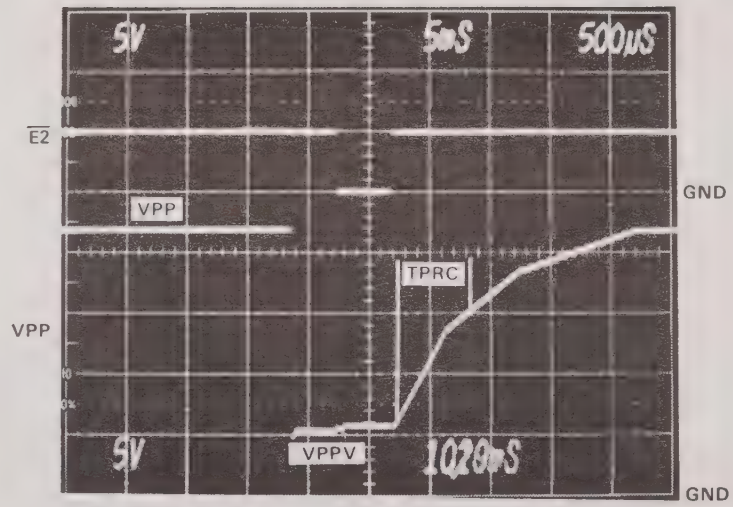
TIMING DIAGRAM

FAMILY CODES 35, 36

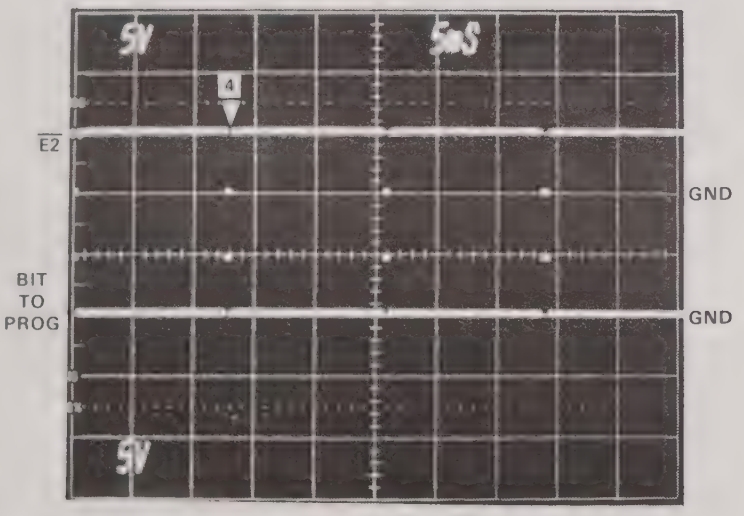
DATA I/O


5V
5mS
2
E2
TPW
GND
VPP
5V
GND

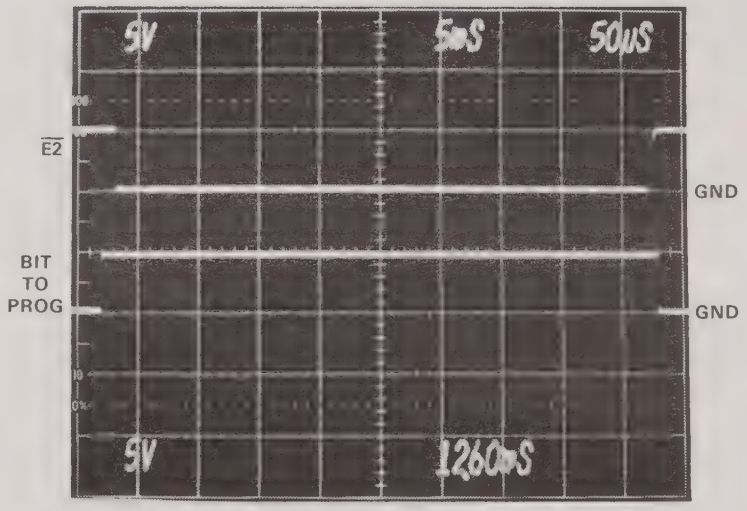
1


5V
5mS
500uS
E2
GND
VPP
TPRC
VPP
5V
VPPV
1029uS
GND

2


5V
5mS
4
E2
GND
BIT
TO
PROG
GND
5V

3


5V
5mS
50uS
E2
GND
BIT
TO
PROG
GND
5V
1260uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.0	5.0	6.0	V	
	VOE	9.0	12.0	15.0	V	
	TPW	9.0	10.0	15.0	ms	
	TPRC	450	600	750	µs	See Note 3
	TF			100	µs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 37.*
2. *Load RAM with hex 01 for Family 38, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *TPRC is measured from 6V to 15.5V.*
4. *Photos 10 and 11 are erase waveforms.*

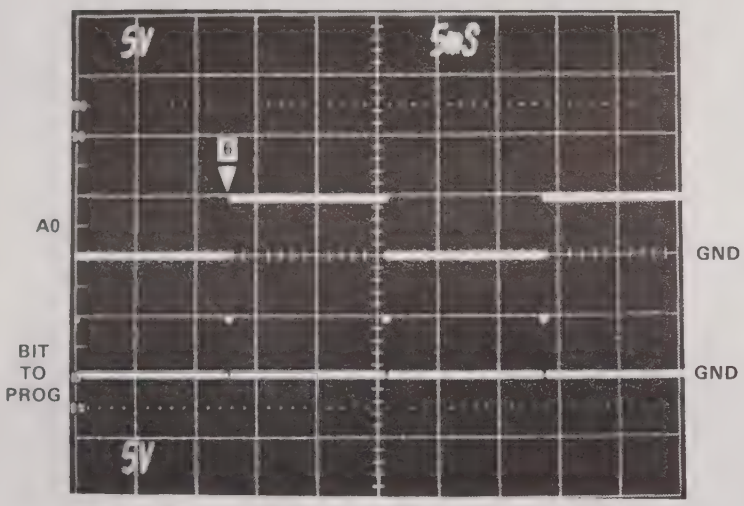
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

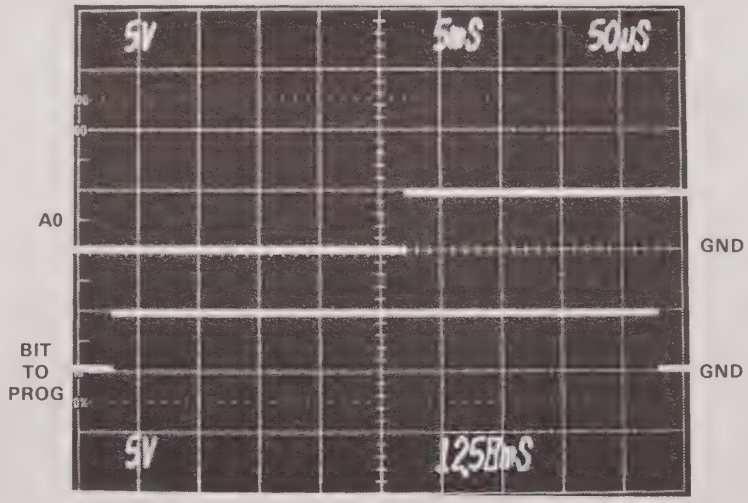
TIMING DIAGRAM

FAMILY CODES 37, 38

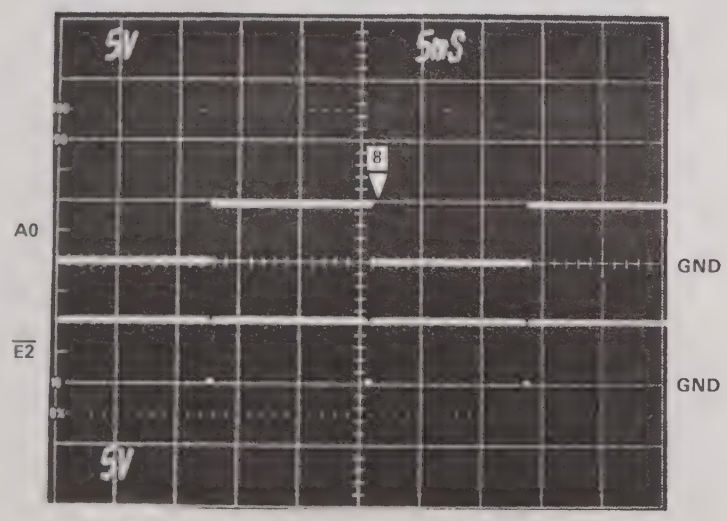
DATA I/O


5V
5mS
6
A0
GND
BIT
TO
PROG
GND
5V

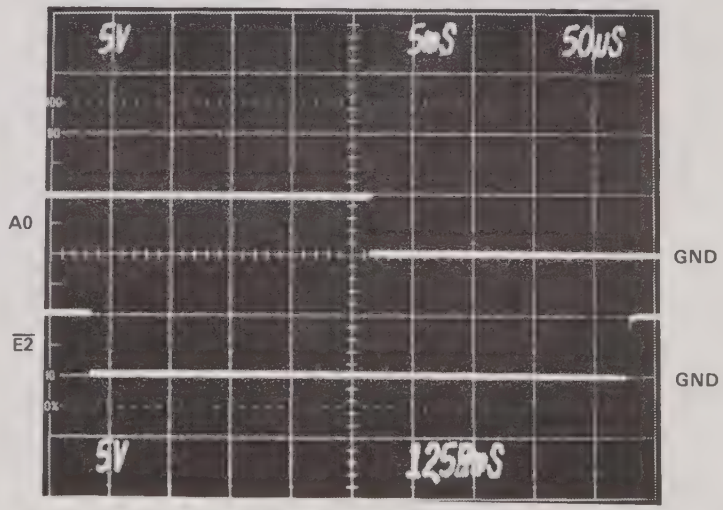
5


5V
5mS
50uS
A0
GND
BIT
TO
PROG
GND
5V
125mS

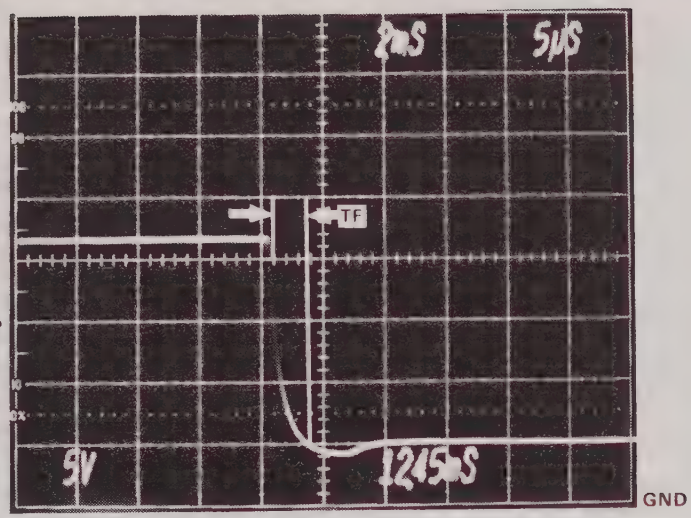
6


5V
5mS
8
A0
GND
E2
GND
5V

7


5V
5mS
50uS
A0
GND
E2
GND
5V
125mS

8



9

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981-0003

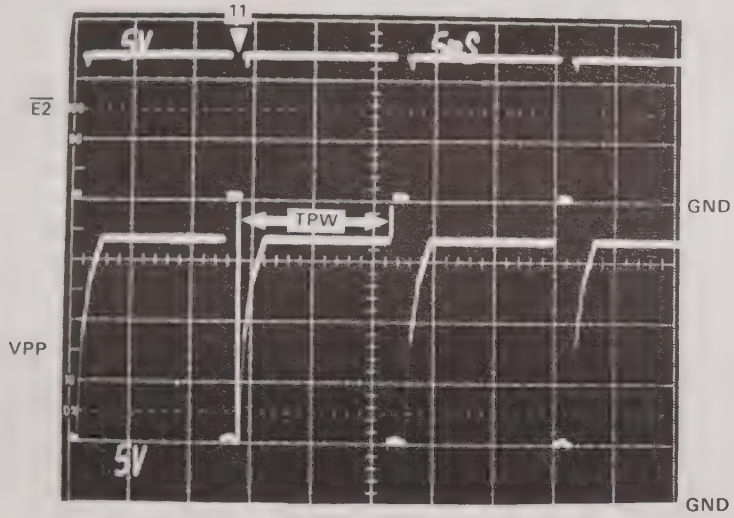
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

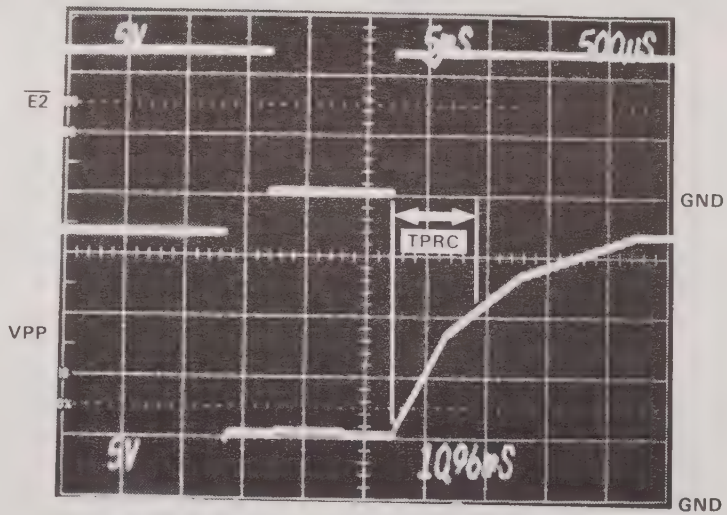
TIMING DIAGRAM

FAMILY CODES 37, 38

DATA I/O


11
5V
5mS
E2
TPW
GND
VPP
5V
GND

10


5V
5mS
500uS
E2
GND
TPRC
VPP
5V
1096mS
GND

11

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981-0003

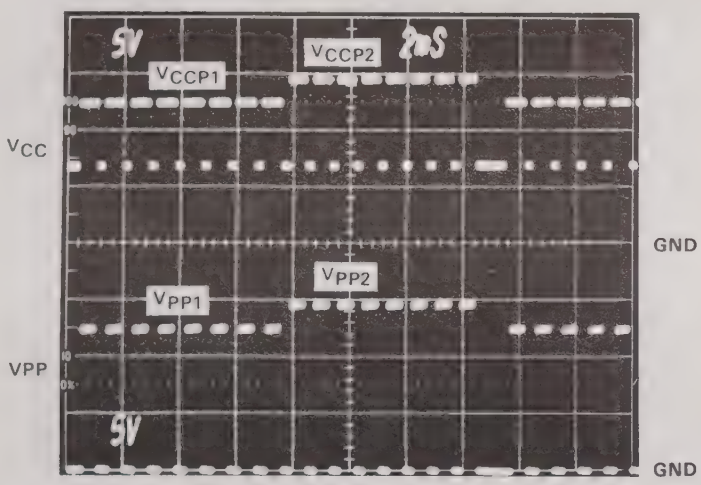
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	C73	3/84

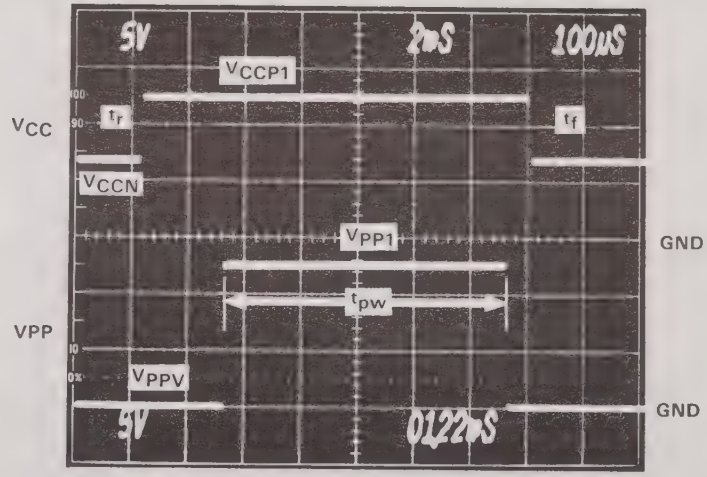
TIMING DIAGRAM

FAMILY CODES 37, 38

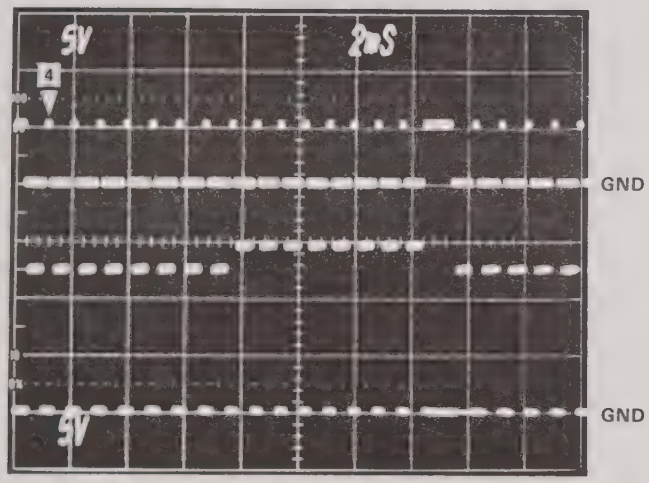
DATA I/O


5V
VCCP1
VCCP2
2mS
VCC
GND
VPP1
VPP2
VPP
5V
GND

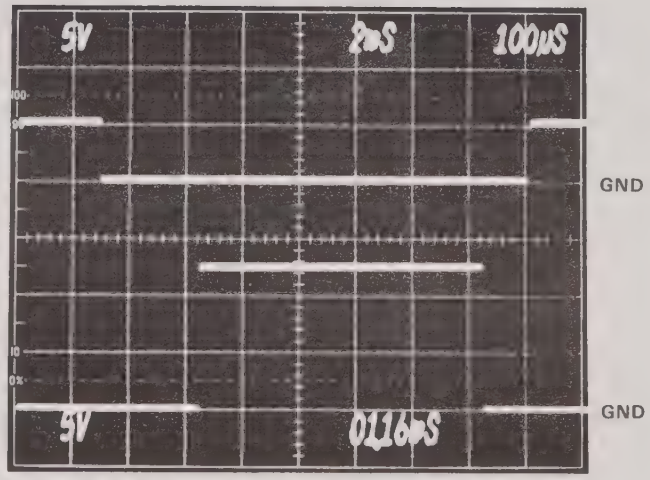
1


5V
2mS
100uS
VCCP1
VCC
tr
tf
VCCN
VPP1
GND
tpw
VPP
VPPV
5V
0122mS
GND

2


5V
2mS
4
E3
GND
VPP
5V
GND

3


5V
2mS
100uS
E3
GND
VPP
5V
0116mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCN}	6.0	6.5	7.0	V	
	V_{CCP1}	11.5	12.0	12.5	V	Pulses 1-8
	V_{CCP2}	13.5	14.0	14.5	V	Pulses 9-16
	V_{PP1}	11.5	12.0	12.5	V	Pulses 1-8
	V_{PP2}	13.5	14.0	14.5	V	Pulses 9-16
	V_{PPV}	0.0		1.0	V	
	V_{OP1}	11.5	12.0	12.5	V	Pulses 1-8
	V_{OP2}	13.5	14.0	14.5	V	Pulses 9-16
	t_{pw}	450	500	550	us	
	t_r	1.0			us	
	t_f	1.0			us	
	Reject		16		PULSES	
	Overprogram		2		PULSES	
1ST PASS VERIFY	V_{CC}	3.9	4.0	4.1	V	
	V_{REF}	0.7	0.8	0.9	V	701-1998/TP4
	HIGH LOAD	5.5	6.5	7.5	V	701-1998/TP2
	LOW LOAD	5.5	6.5	7.5	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	4.0	4.1	4.2	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	8.8	9.8	10.8	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 39.*
2. *Load RAM with hex 01 for Family 40.*
3. *V_{CC} is loaded with a 100 Ω, 2-watt resistor.*

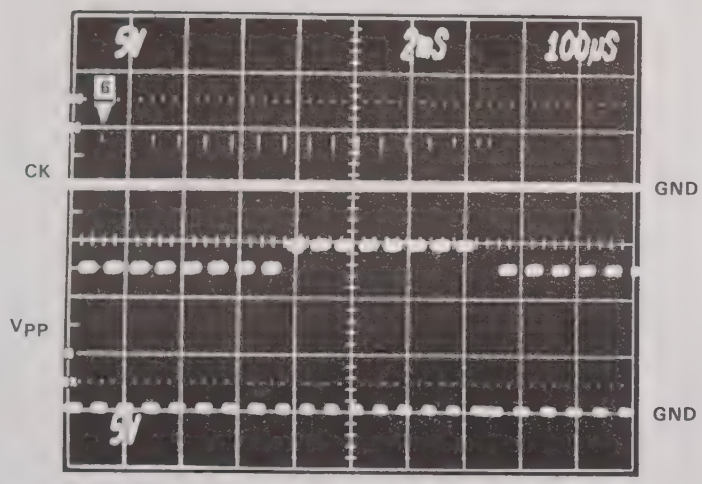
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	C78	3/84

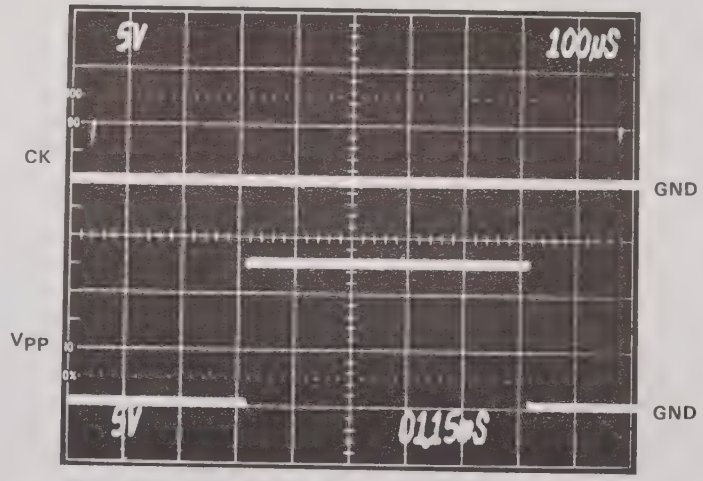
TIMING DIAGRAM

FAMILY CODES 39, 40

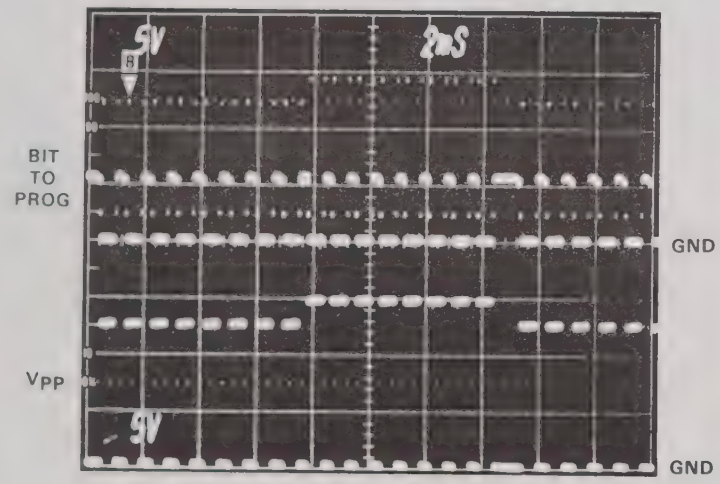
DATA I/O


5V
2mS
100µS
CK
GND
VPP
GND
5V

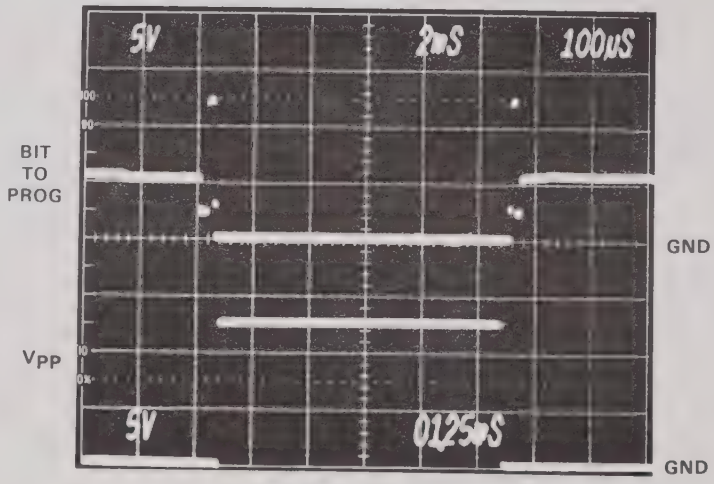
5


5V
100µS
CK
GND
VPP
GND
5V
0115mS

6


5V
2mS
BIT
TO
PROG
GND
VPP
5V
GND

7


5V
2mS
100µS
BIT
TO
PROG
GND
VPP
5V
0125mS
GND

8

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981-0003

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

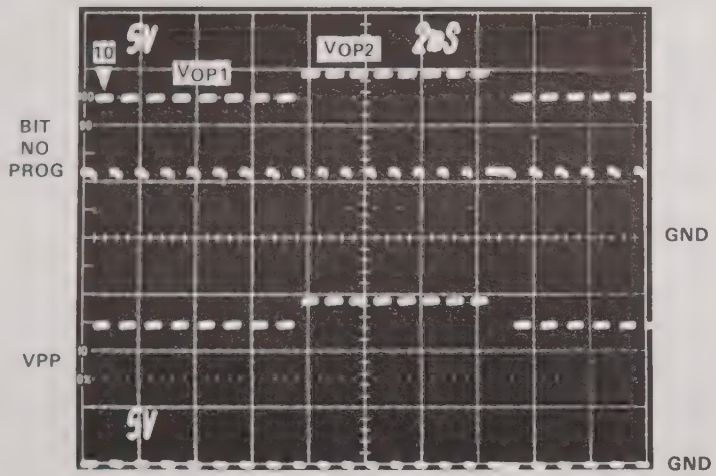
Sheet 2 of 3

TIMING DIAGRAM

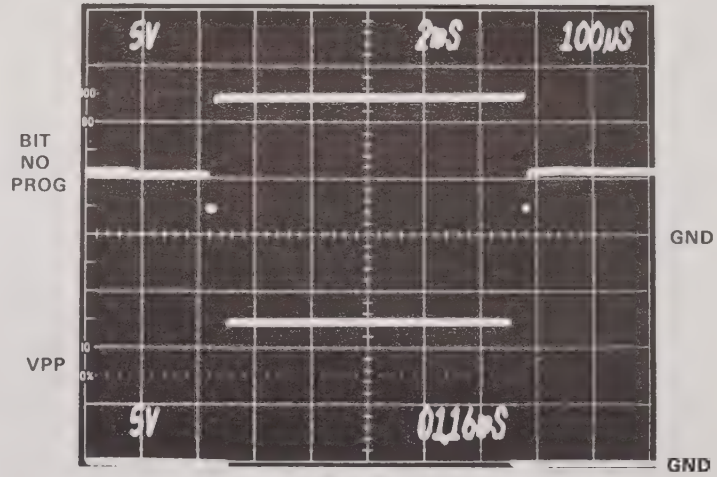
FAMILY CODES 39, 40

DATA I/O

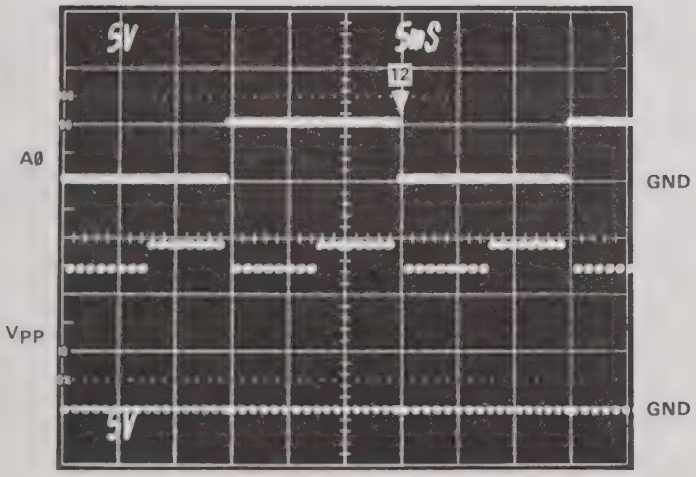
0526 1282


5V
10
VOP1
VOP2
2mS
BIT
NO
PROG
GND
VPP
5V
GND

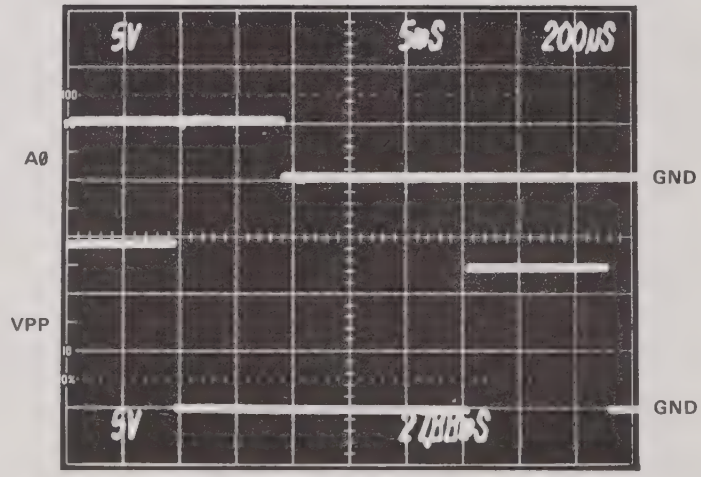
9


5V
2mS
100µS
BIT
NO
PROG
GND
VPP
5V
GND

10


5V
5mS
12
A0
GND
VPP
5V
GND

11


5V
5mS
200µS
A0
GND
VPP
5V
GND

12

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

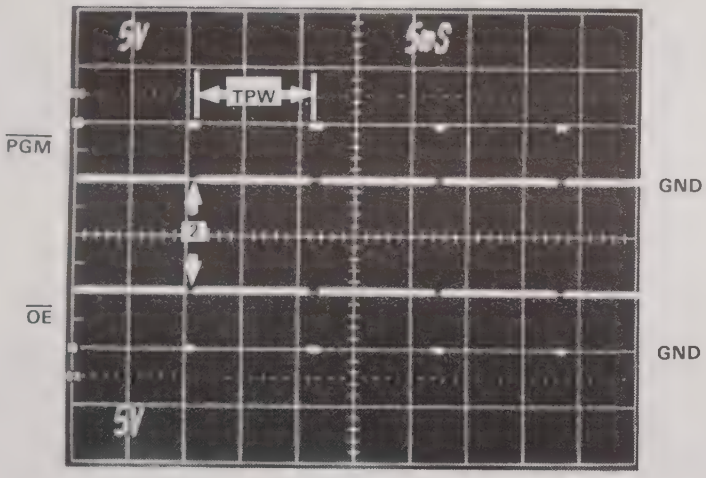
Sheet 3 of 3

TIMING DIAGRAM

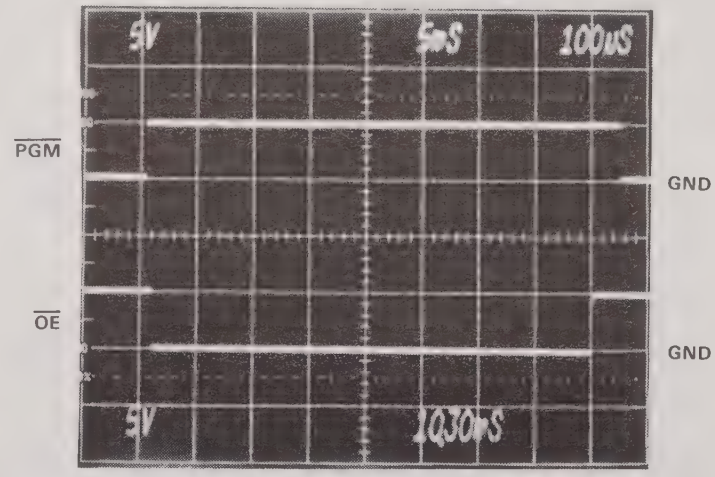
FAMILY CODES 39, 40

DATA I/O

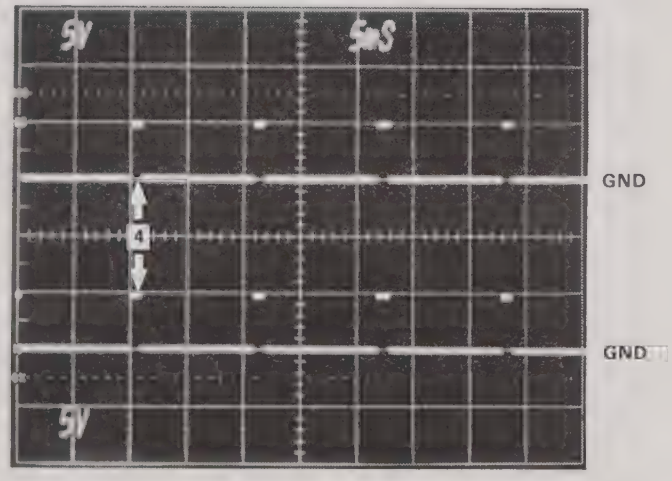
0526/1282


5V
5mS
TPW
PGM
GND
2
OE
GND
5V

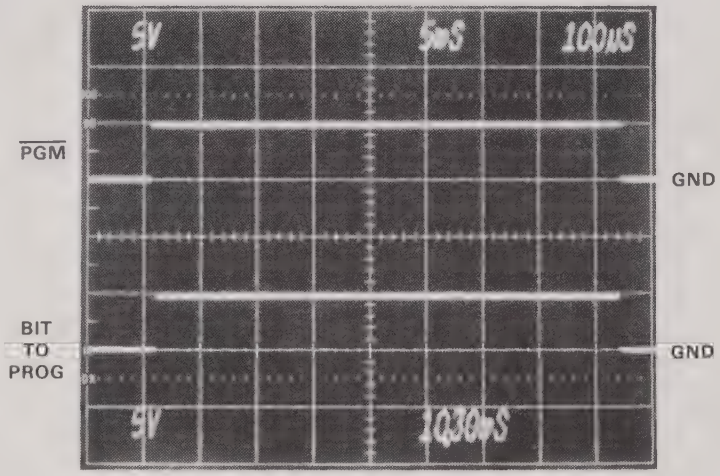
1


5V
5mS
100uS
PGM
GND
OE
GND
5V
1Q30mS

2


5V
5mS
PGM
GND
4
BIT
TO
PROG
GND
5V

3


5V
5mS
100uS
PGM
GND
BIT
TO
PROG
GND
5V
1Q30mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VPP	12.0	12.5	13.0	V	Not Shown
	TPW	9.5	10.0	10.5	ms	
	Reject		1		Pulse	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	3.9	4.9	5.9	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 3B.*
2. *Load RAM with hex 01 for Family 3C.*

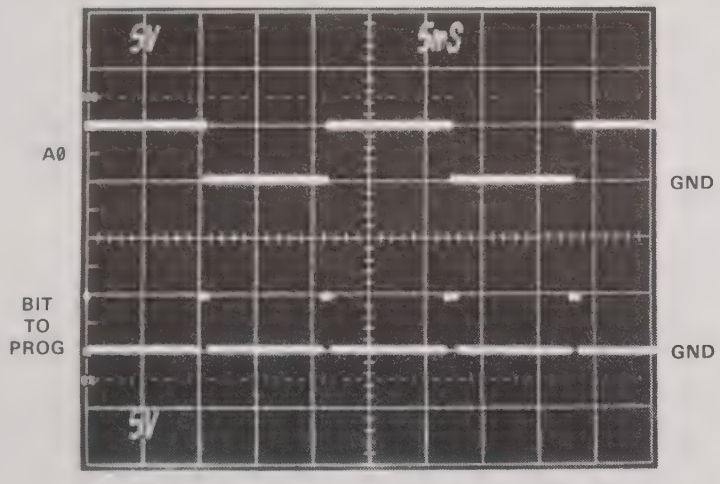
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

TIMING DIAGRAM

FAMILY CODES 3B, 3C

DATA I/O



5

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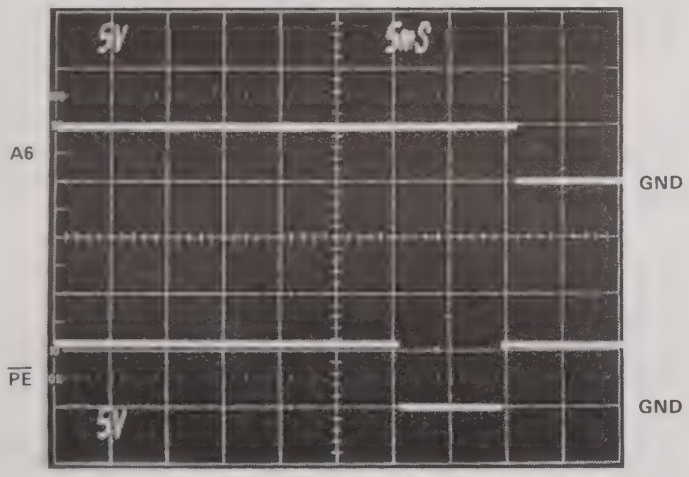
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

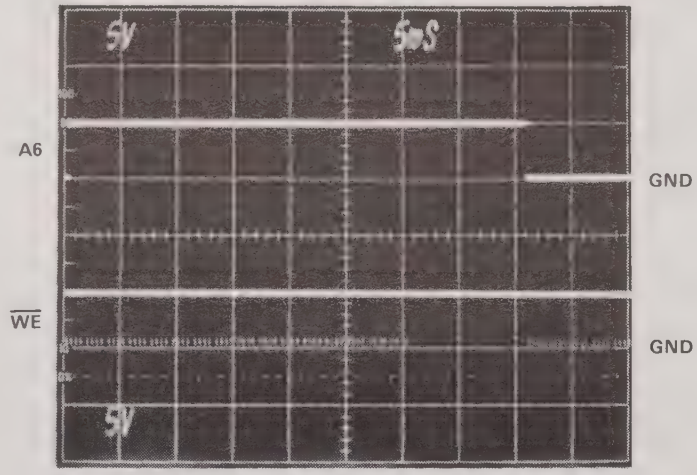
TIMING DIAGRAM

FAMILY CODES 3B, 3C

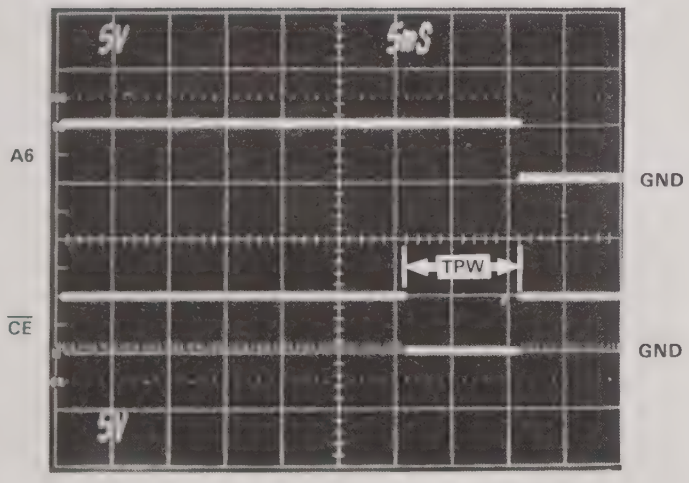
DATA I/O


5V
5mS
A6
GND
PE
GND
5V

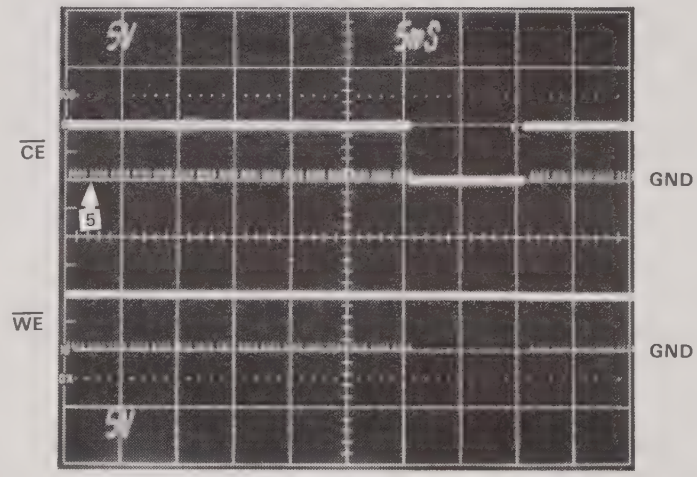
1


5V
5mS
A6
GND
WE
GND
5V

2


5V
5mS
A6
GND
TPW
CE
GND
5V

3


5V
5mS
CE
GND
5
WE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	TPW	10.0			ms	
	TEW	100			ms	
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	3.9	4.9	5.9	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 3D.*
2. *Load RAM with hex 01 for Family 3E.*
3. *Photos 6 and 7 show erase pulse.*

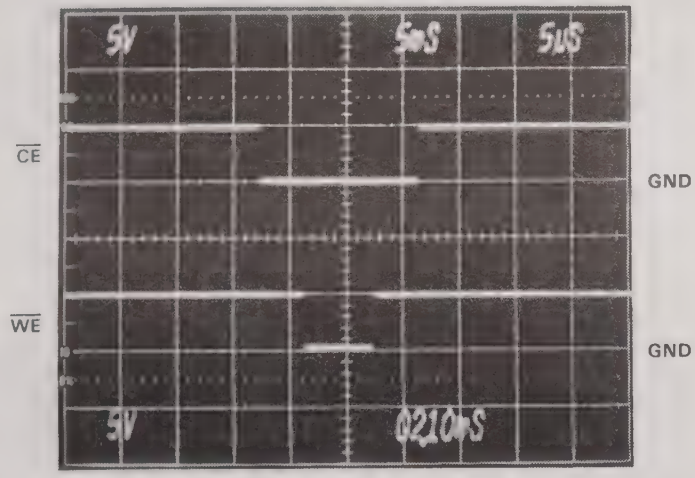
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

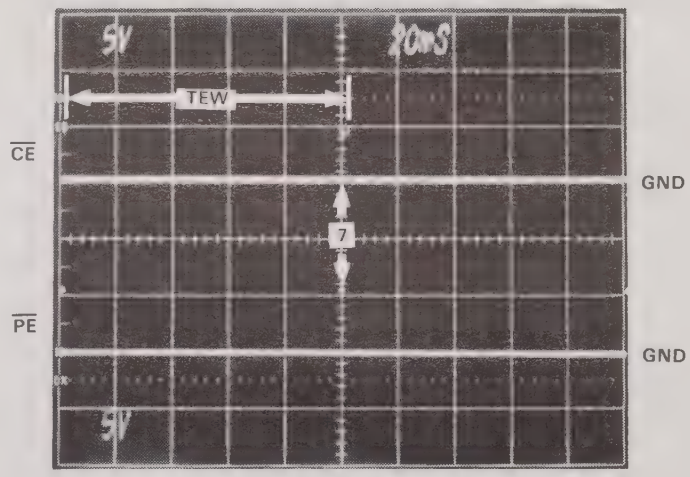
TIMING DIAGRAM

FAMILY CODES 3D, 3E

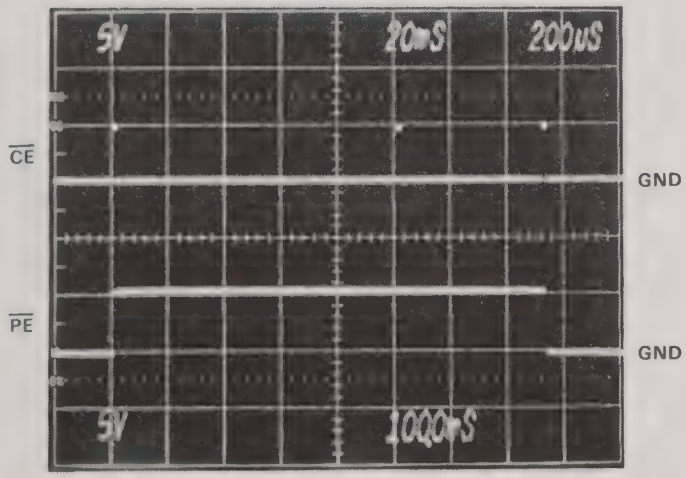
DATA I/O


5V
5mS
5uS
CE
GND
WE
GND
5V
0210mS

5


5V
20mS
TEW
CE
GND
7
PE
GND
5V

6


5V
20mS
200uS
CE
GND
PE
GND
5V
1000mS

7

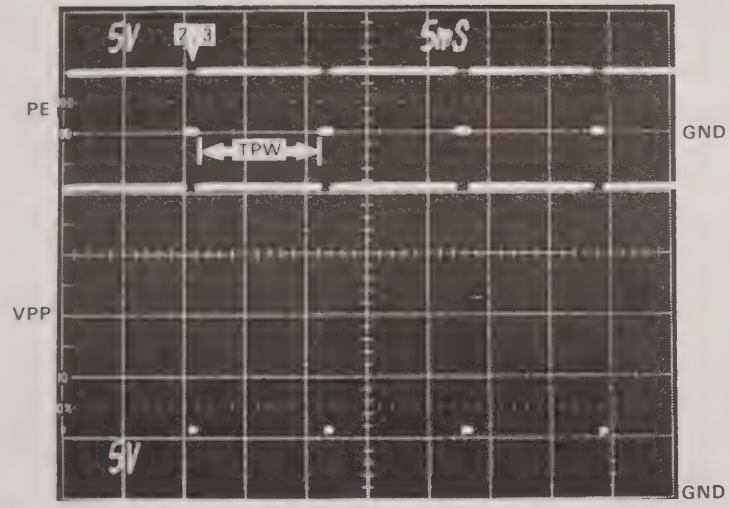
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

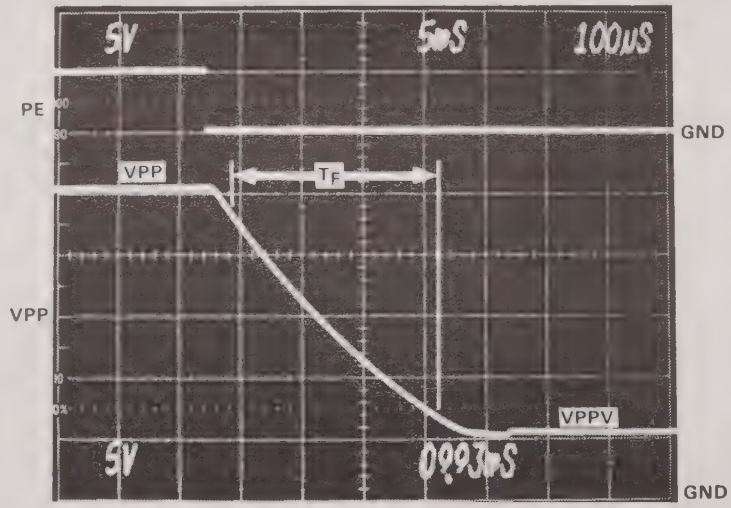
TIMING DIAGRAM

FAMILY CODES 3D, 3E

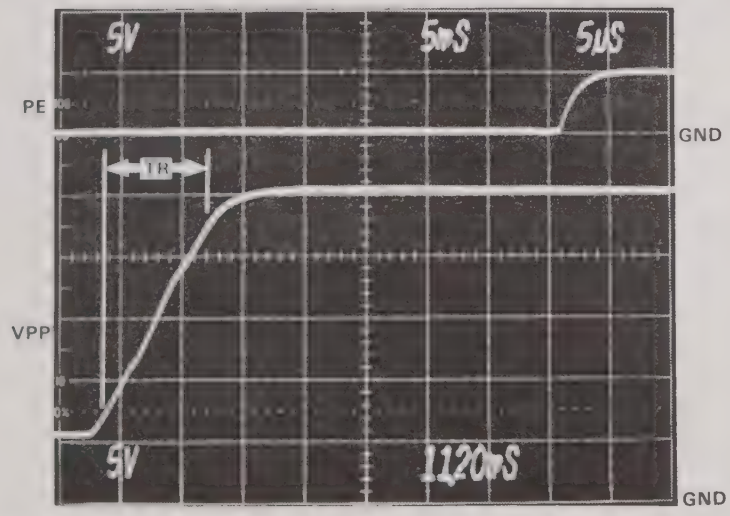
DATA I/O


5V
2
3
5mS
PE
GND
TPW
VPP
5V
GND

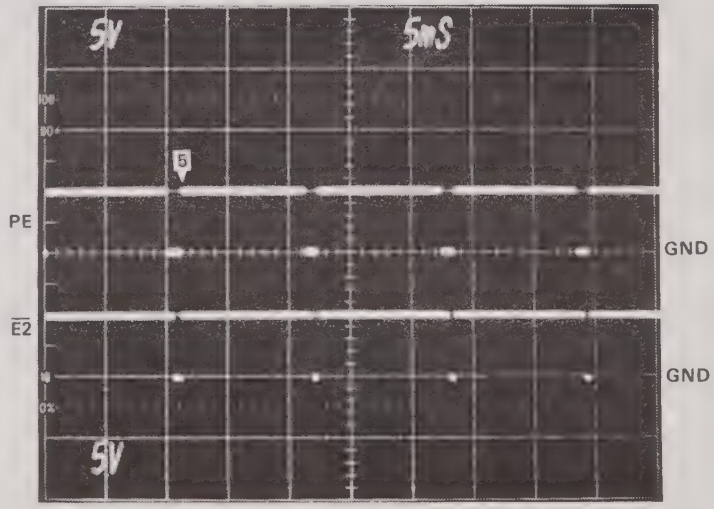
1


5V
5mS
100uS
PE
GND
VPP
TF
VPP
VPPV
5V
0.993mS
GND

2


5V
5mS
5uS
PE
GND
TR
VPP
5V
1120mS
GND

3


5V
5mS
5
PE
GND
E2
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.00	5.25	V	
	TPW	9.8	10.0	10.2	ms	
	TR	50			ns	
	TEP	98	100	102	ms	
	TF	50			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 43.*
2. *Load RAM with hex 01 for Family 44, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photo 10 is the erase waveform.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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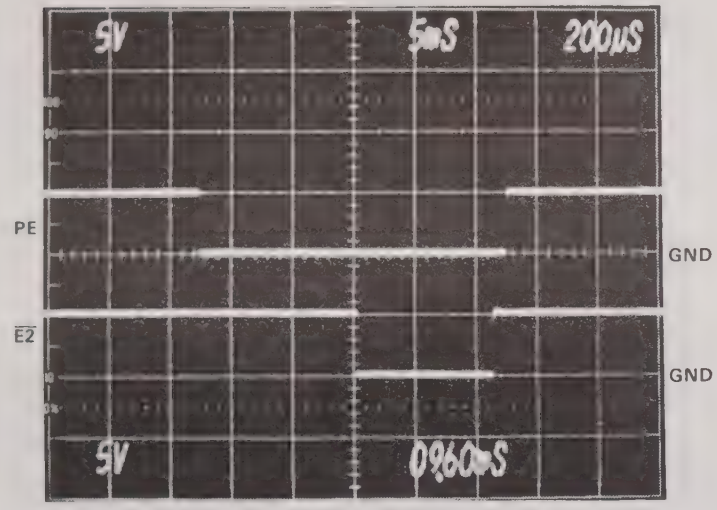
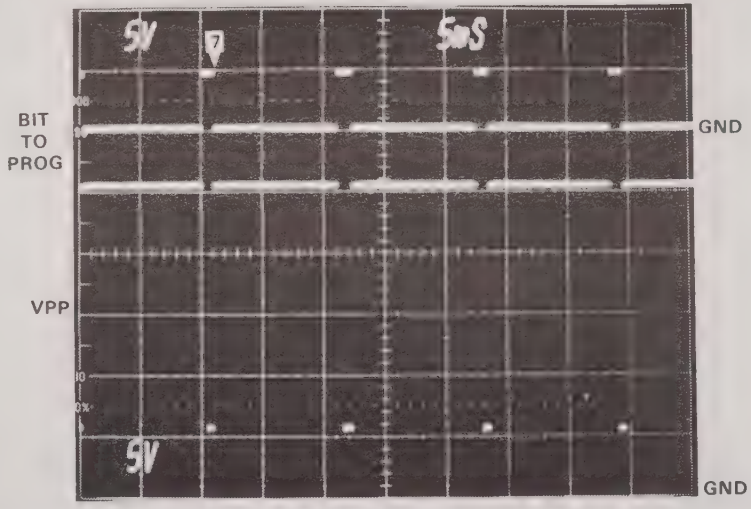
TIMING DIAGRAM

FAMILY CODES 43, 44

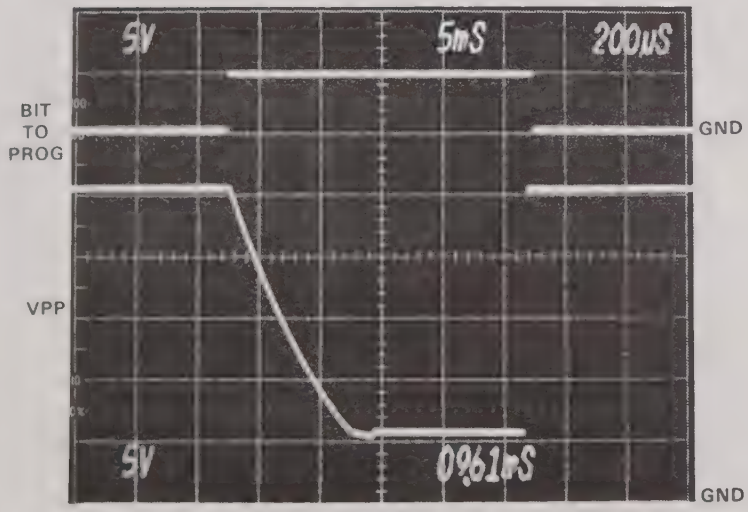
DATA I/O


5V
5mS
200uS
PE
GND
E2
GND
5V
0%60mS

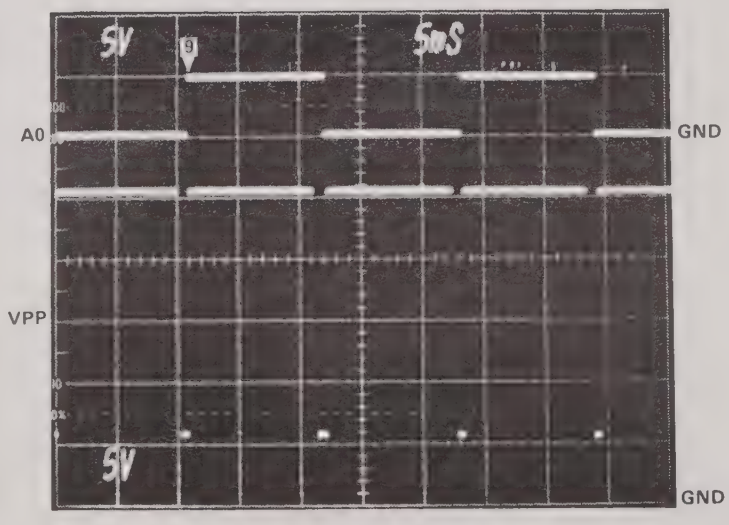
5


5V
7
5mS
BIT
TO
PROG
GND
VPP
5V
GND

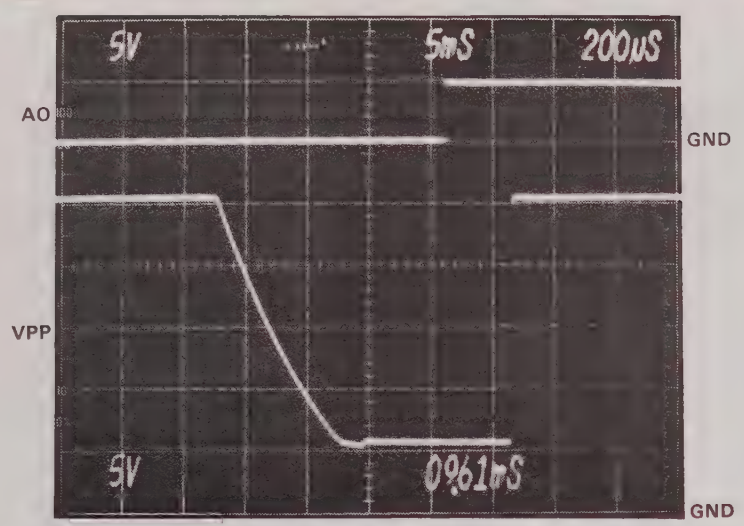
6


5V
5mS
200uS
BIT
TO
PROG
GND
VPP
5V
0%61mS
GND

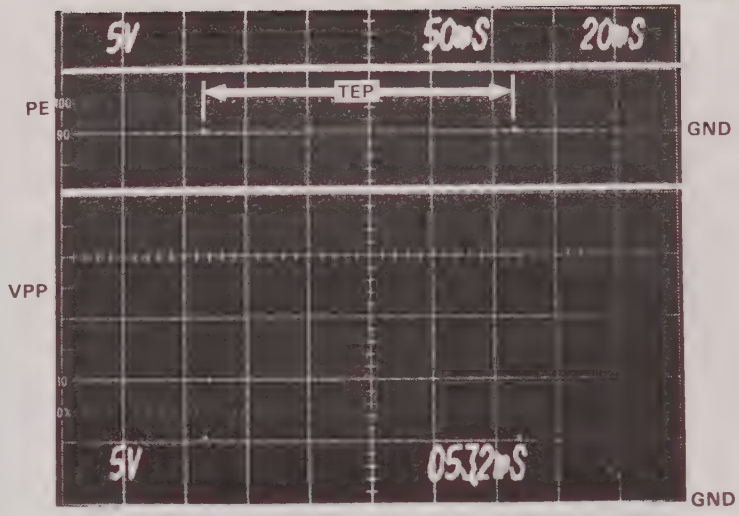
7


5V
9
5mS
A0
GND
VPP
5V
GND

8



9



10

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

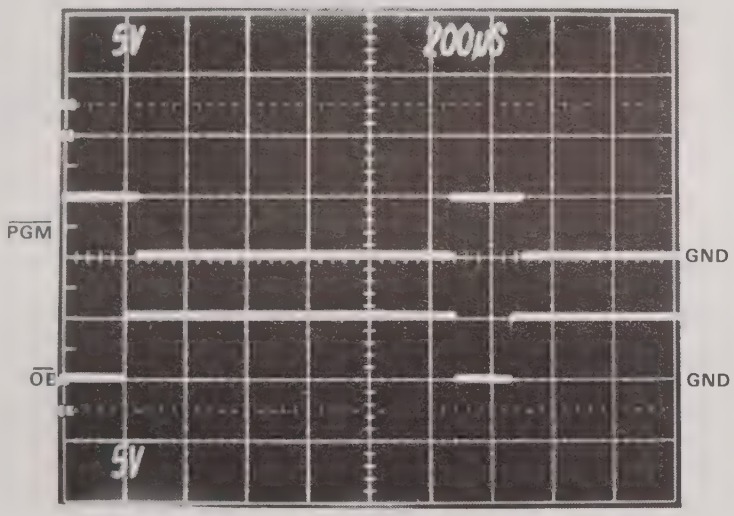
Sheet 2 of 2

TIMING DIAGRAM

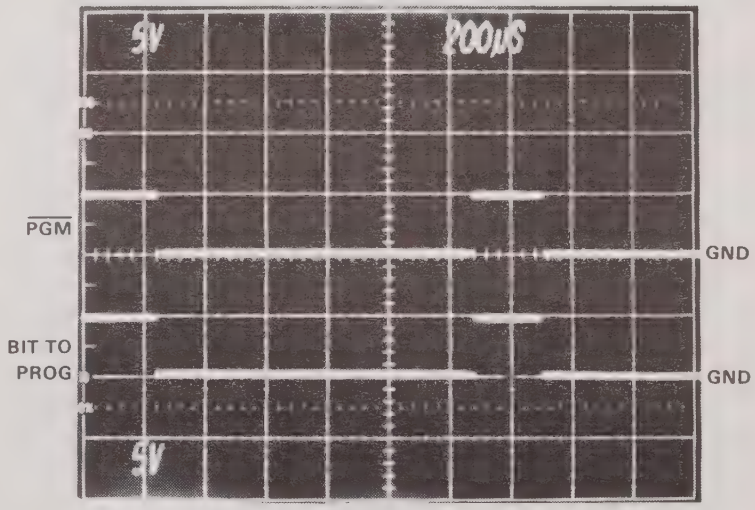
FAMILY CODES 43, 44

DATA I/O

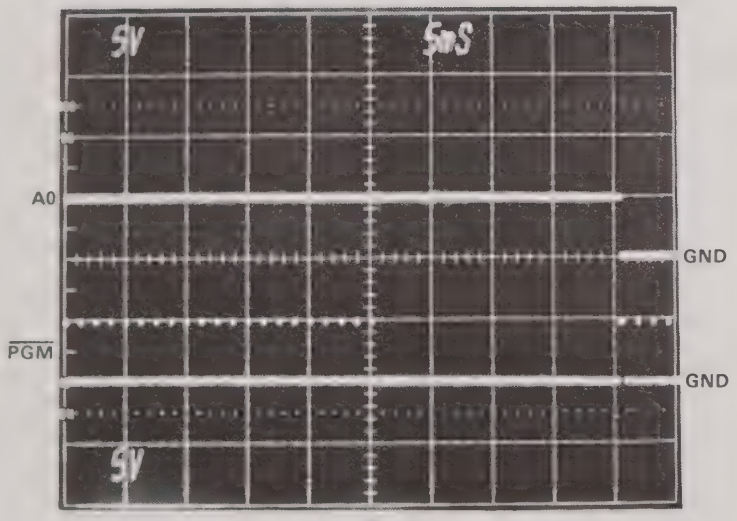
0526 1282


5V
200µS
PGM
GND
OE
GND
5V

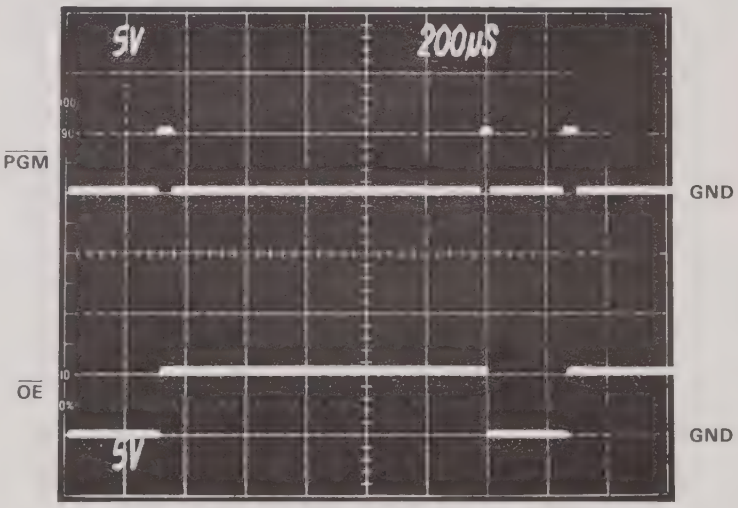
1


5V
200µS
PGM
GND
BIT TO
PROG
GND
5V

2


5V
5mS
A0
GND
PGM
GND
5V

3


5V
200µS
PGM
GND
OE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.00	6.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	Not shown
	VPPV					NA
	TPW	0.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		20		Pulses	
	Overprogram		1		Pulse	See note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 45.*
2. *Load RAM with hex 01 for Family 46 and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 1 ms times the number of programming pulses required to program the location.*
4. *Photo 4 is for Pinout 32.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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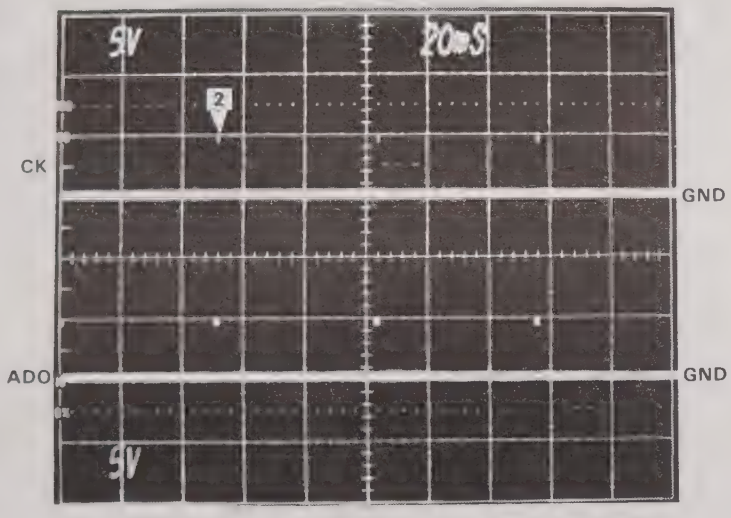
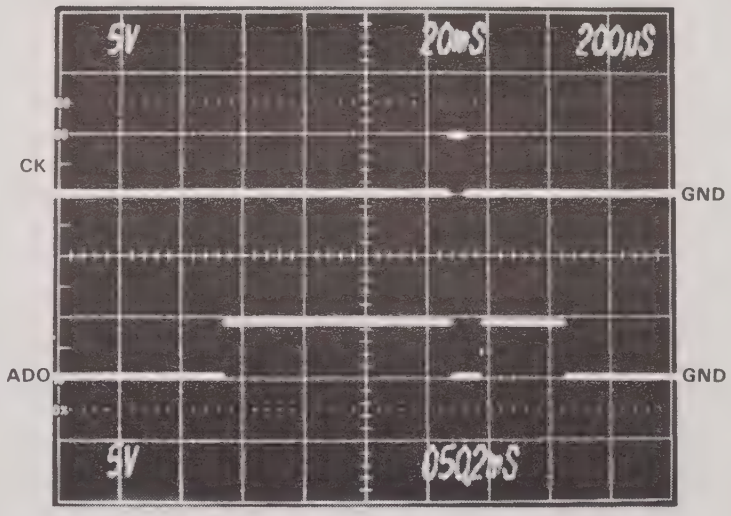
TIMING DIAGRAM

FAMILY CODES 45, 46

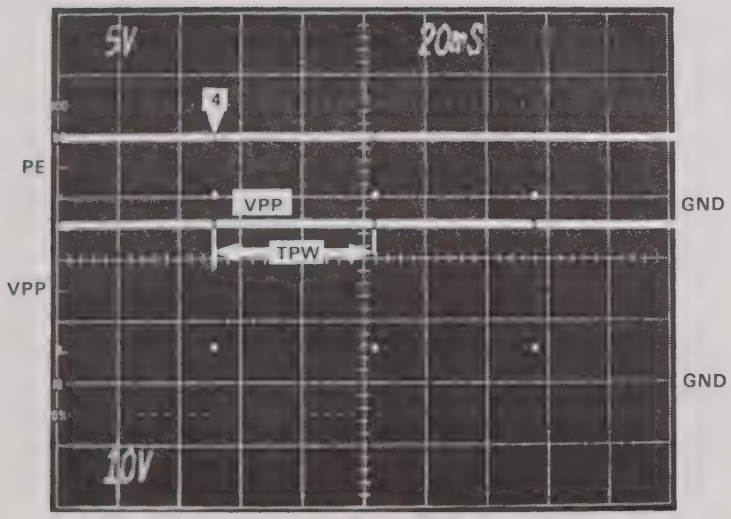
DATA I/O


5V
20mS
2
CK
GND
ADO
GND
5V

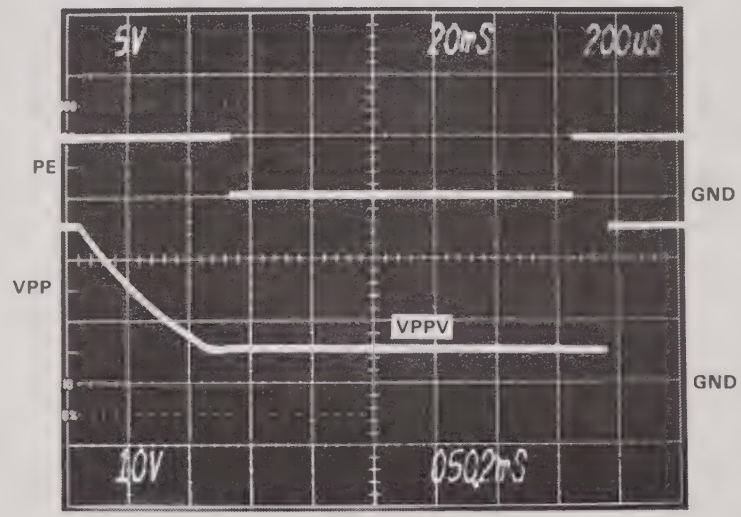
1


5V
20mS
200uS
CK
GND
ADO
GND
5V
0502mS

2


5V
20mS
4
PE
VPP
TPW
GND
VPP
GND
10V

3


5V
20mS
200uS
PE
GND
VPP
VPPV
GND
10V
0502mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not shown
	VOP					NA
	VPP	24.5	25.0	25.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0 0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 47.*
2. *Load RAM with hex 01 for Family 48 and bit-to-prog waveform becomes bit-no-prog waveform.*

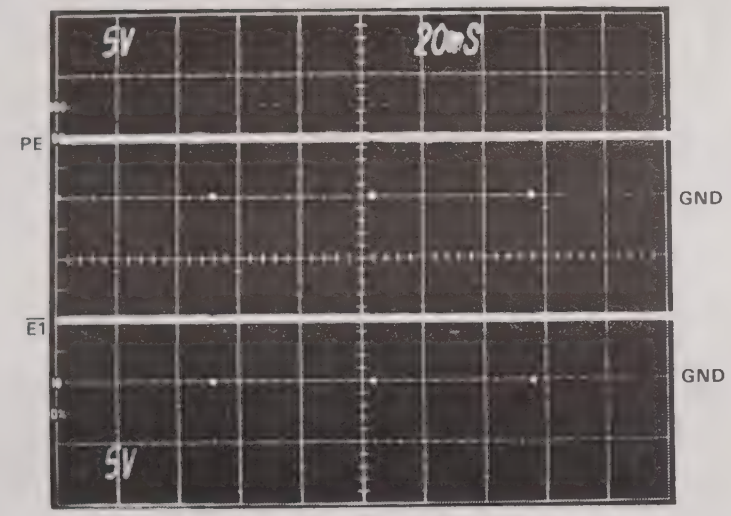
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

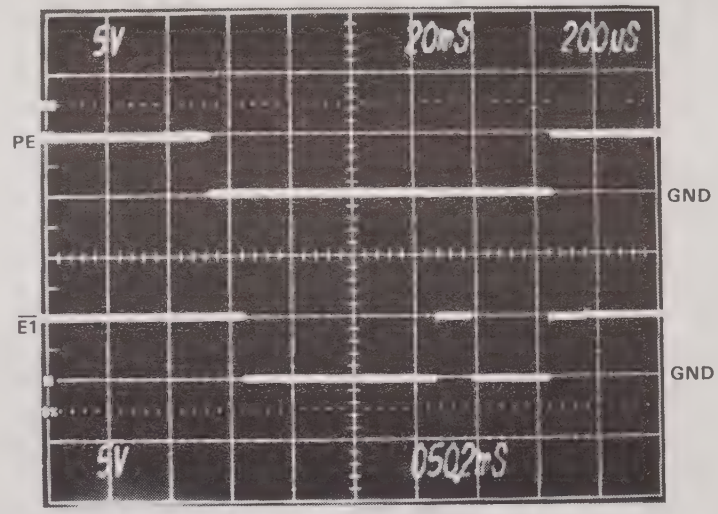
TIMING DIAGRAM

FAMILY CODES 47, 48

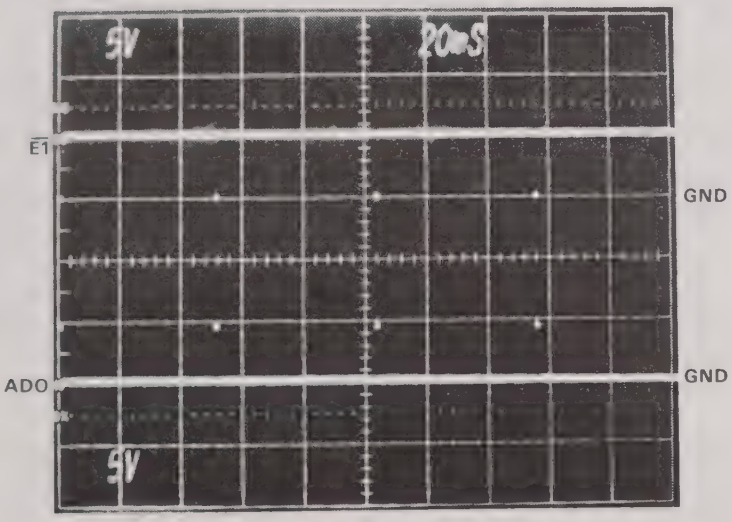
DATA I/O


5V
20mS
PE
GND
E1
GND
5V

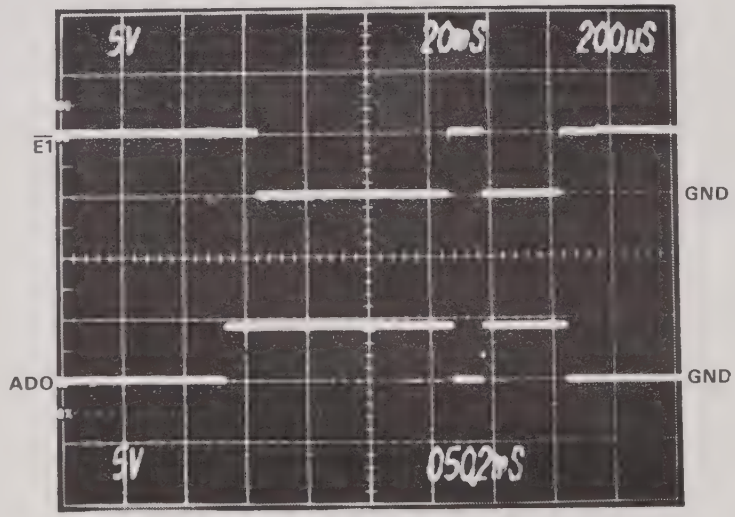
5


5V
20mS
200uS
PE
GND
E1
GND
5V
0502mS

6


5V
20mS
E1
GND
ADO
GND
5V

7


5V
20mS
200uS
E1
GND
ADO
GND
5V
0502mS

8

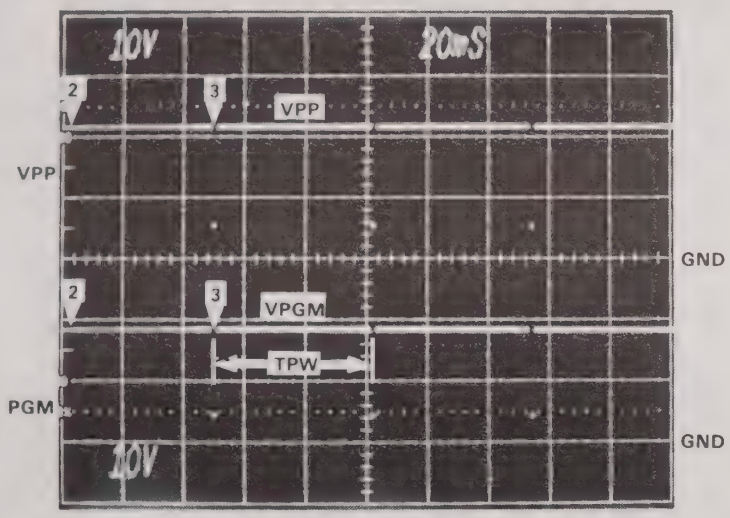
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

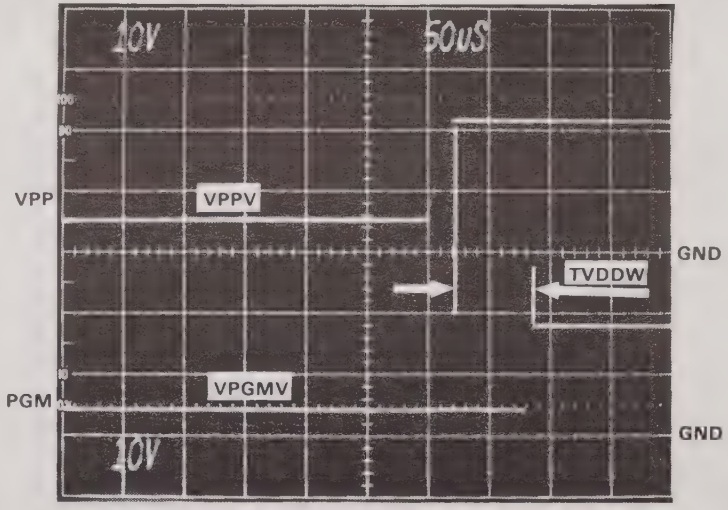
TIMING DIAGRAM

FAMILY CODES 47, 48

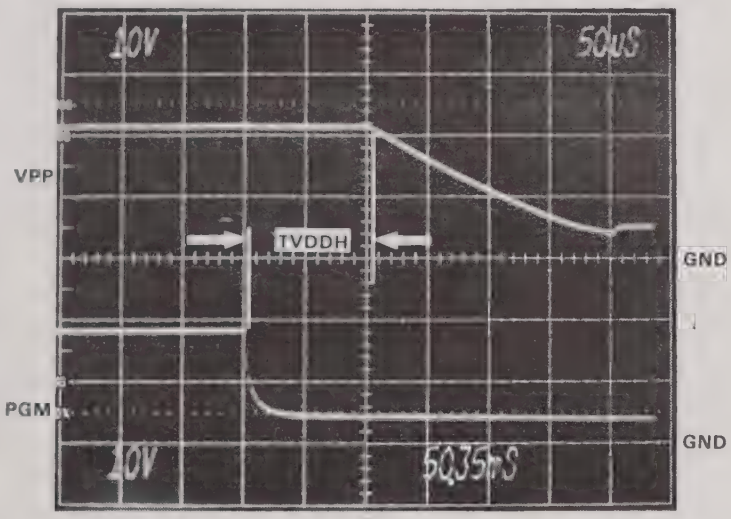
DATA I/O


10V
20mS
2
3
VPP
VPP
GND
2
3
VPGM
TPW
PGM
GND
10V

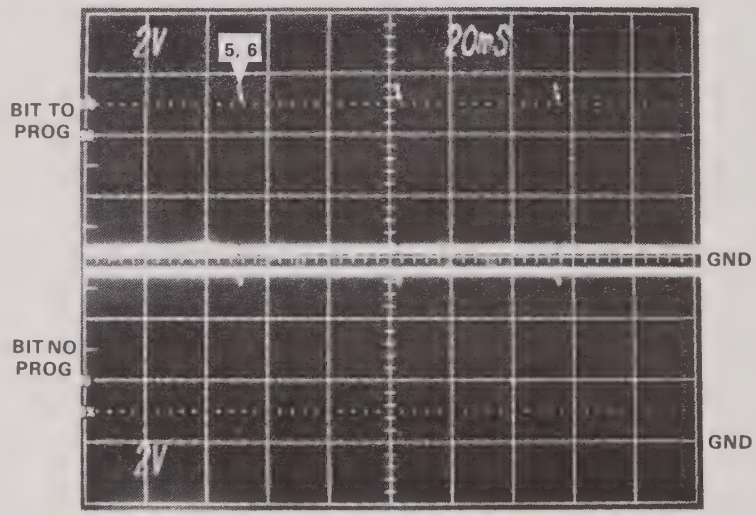
1


10V
50uS
VPP
VPPV
GND
TVDDW
PGM
VPGMV
GND
10V

2


10V
50uS
VPP
TVDDH
GND
PGM
GND
10V
50.35mS

3


2V
5, 6
20mS
BIT TO PROG
GND
BIT NO PROG
GND
2V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.9	5.0	5.1	V	Not shown
	VEA	17.5	18.0	18.5	V	Not shown
	VPP	20.5	21.0	21.5	V	
	VPPV	4.8	5.0	5.2	V	
	VPGM	17.5	18.0	18.5	V	
	VPGMV	4.0		5.1	V	
	TVDDW	0		1.0	ms	
	TVDDH	0		1.0	ms	
	TPW	50		60	ms	
	TWW	17			µs	See note 3
	TAW	17			µs	See note 3
	TWA	17			µs	See note 3
	Reject Overprogram		1 0		Pulse Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.4	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 49*
2. *Load RAM with hex 01 for Family 50 and bit-to-prog waveform becomes bit-no-prog waveform and vice versa.*
3. *4TCY = 17 µs @ 3.579545 MHz.*

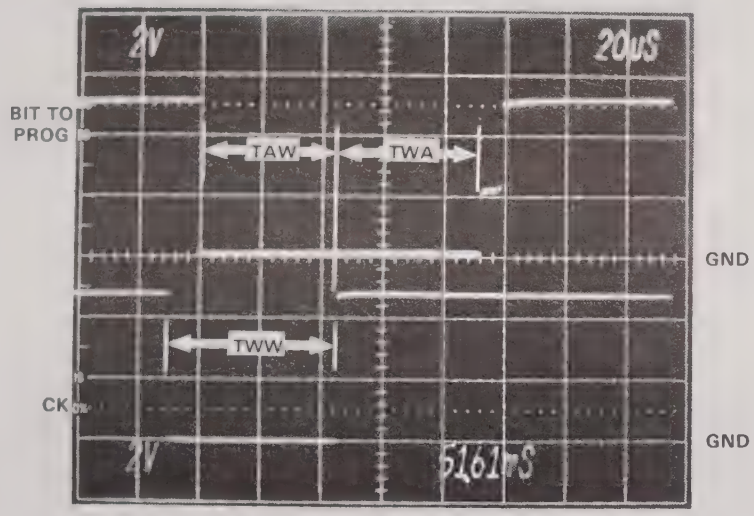
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

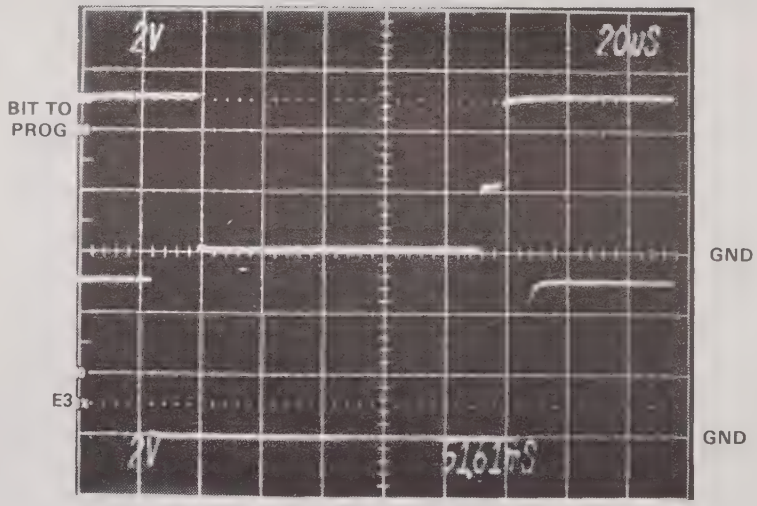
TIMING DIAGRAM

FAMILY CODES 49, 50

DATA I/O


2V
20uS
BIT TO PROG
TAW
TWA
GND
TWW
CK
2V
5161mS
GND

5


2V
20uS
BIT TO PROG
GND
E3
2V
5161mS
GND

6

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

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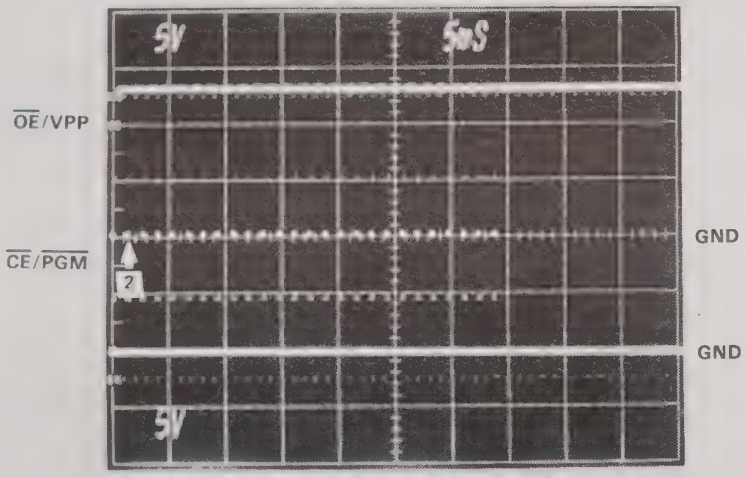
TIMING DIAGRAM

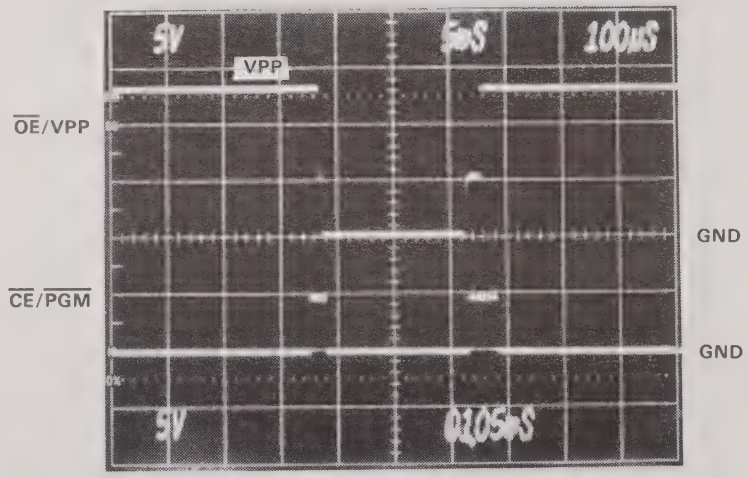
FAMILY CODES 49, 50

DATA I/O

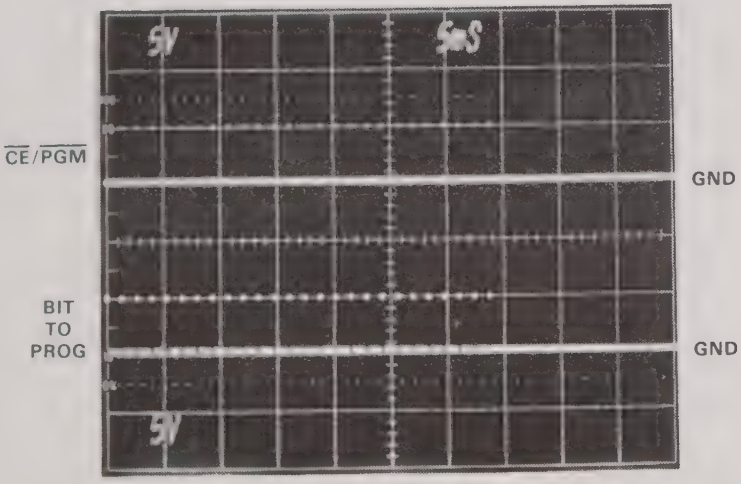
0526/1282


5V
5mS
OE/VPP
CE/PGM
2
GND
GND
5V

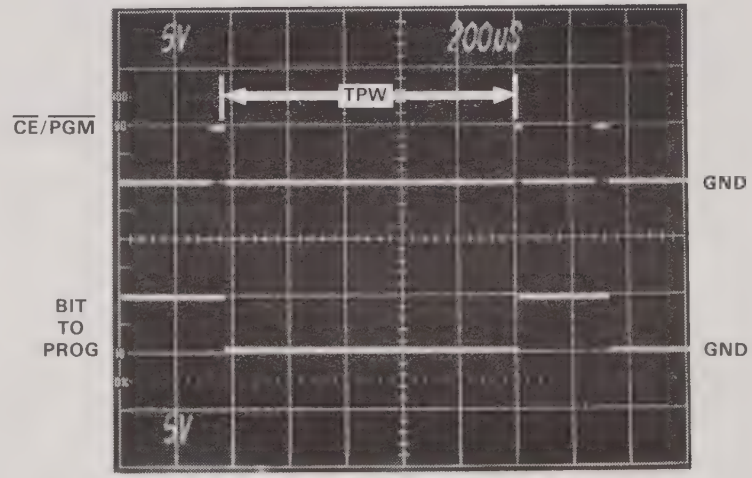
1


5V
5mS
100uS
VPP
OE/VPP
GND
CE/PGM
GND
5V
0105mS

2


5V
5mS
CE/PGM
GND
BIT
TO
PROG
GND
5V

3


5V
200uS
TPW
CE/PGM
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	Not Shown
	VPP	12.0	12.5	13.0	V	
	TPW	0.95	1.0	1.05	ms	
	Reject		25		Pulses	
	Overprogram		1			See Note 3
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	3.9	4.9	5.9	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 4B.*
2. *Load RAM with hex 01 for Family 4C.*
3. *The overprogram pulse is 3 ms times the number of programming pulses required to program the location.*

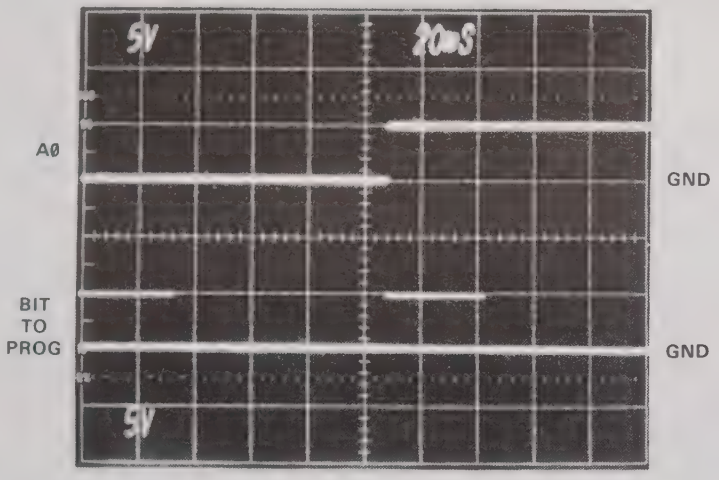
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

TIMING DIAGRAM

FAMILY CODES 4B, 4C

DATA I/O



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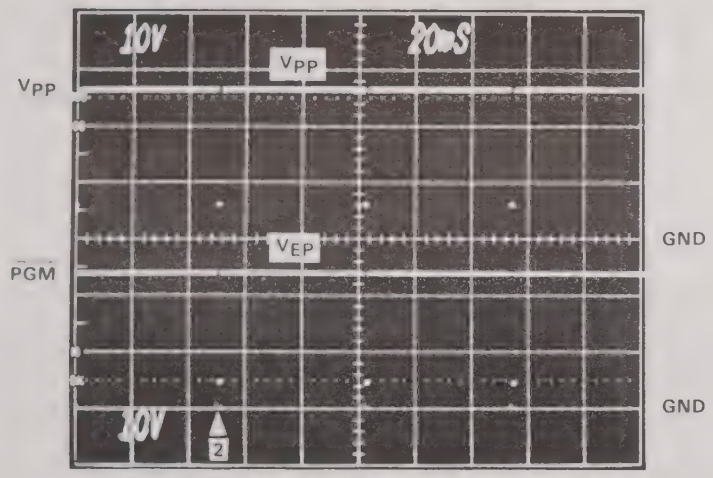
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

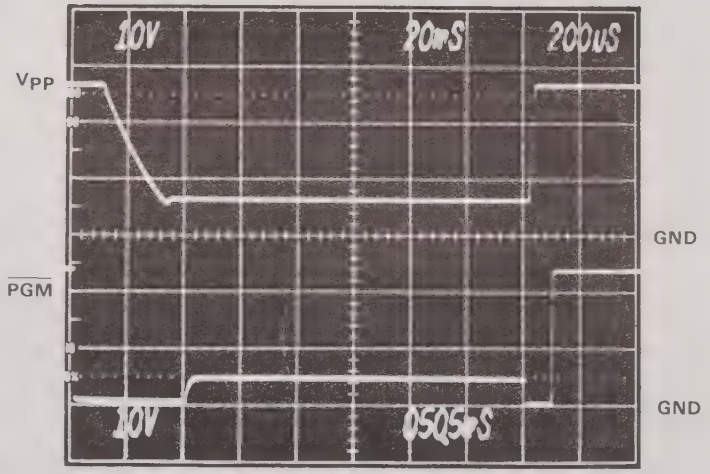
TIMING DIAGRAM

FAMILY CODES 4B, 4C

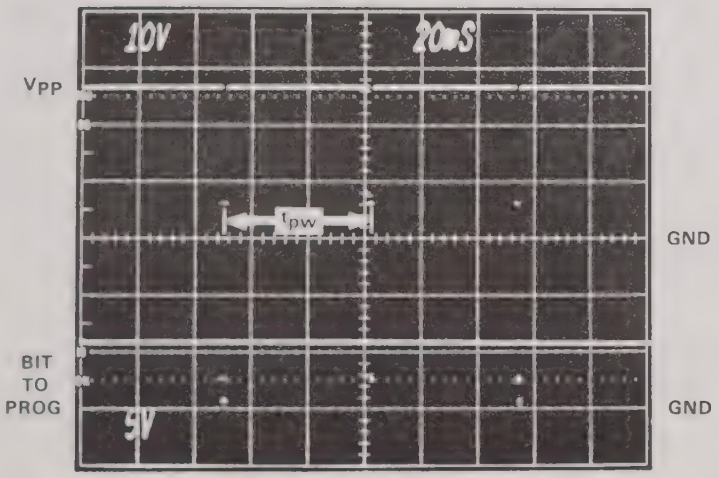
DATA I/O


10V
20mS
VPP
VPP
VEP
GND
PGM
GND
10V
2

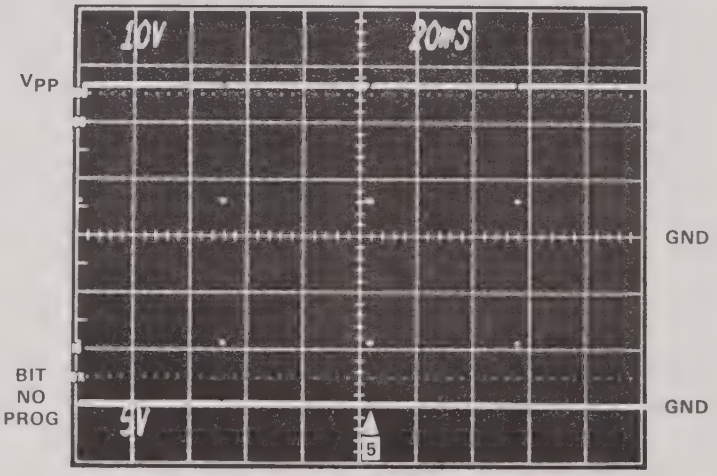
1


10V
20mS
200uS
VPP
GND
PGM
GND
10V
0505mS

2


10V
20mS
VPP
tpw
GND
BIT
TO
PROG
GND
9V

3


10V
20mS
VPP
GND
BIT
NO
PROG
GND
9V
5

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	24.0	25.0	26.0	V	
	V_{PPV}					N.A.
	V_{EP}	21.5	23.0	24.5	V	
	t_{pw}	49	50	51	ms	
	t_r					N.A.
	t_{ww}	20			μs	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		1		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 51.*
2. *Load RAM with hex 01 for Family 52.*

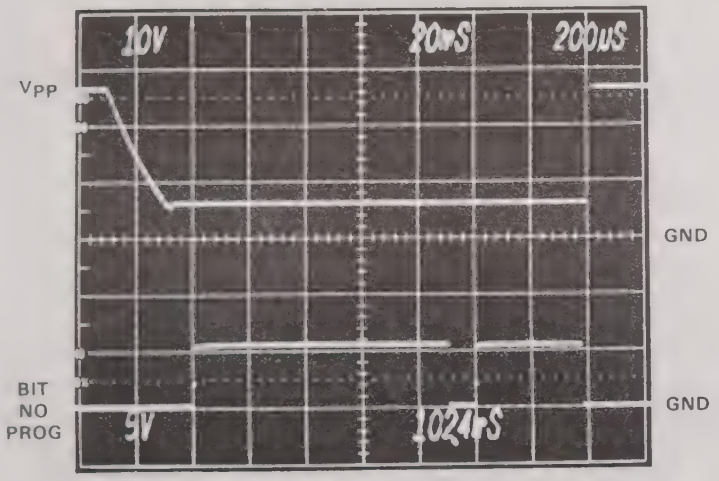
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

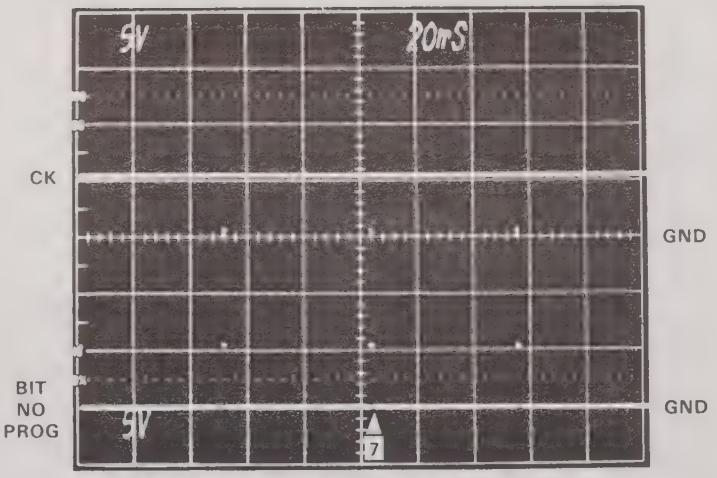
TIMING DIAGRAM

FAMILY CODES 51, 52

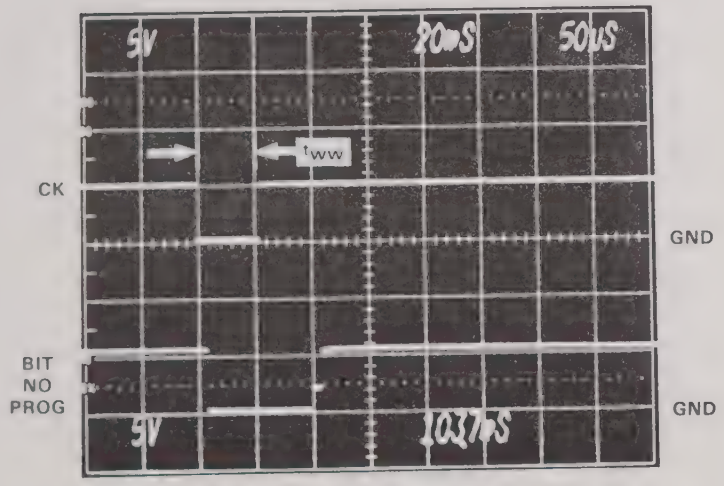
DATA I/O


10V
20mS
200uS
VPP
GND
BIT
NO
PROG
5V
1024mS
GND

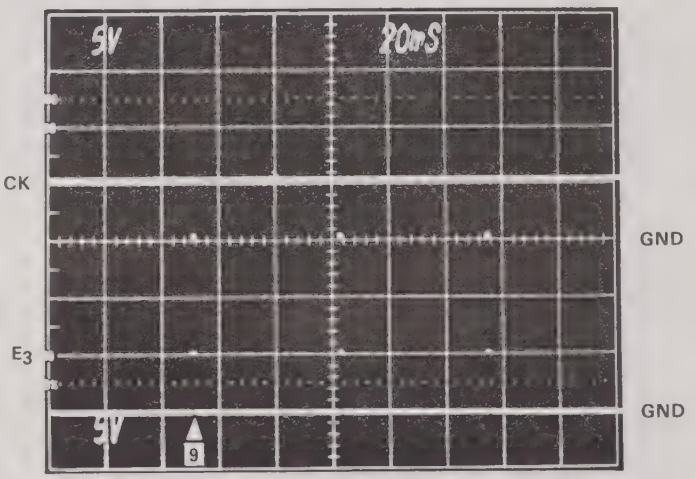
5


5V
20mS
CK
GND
BIT
NO
PROG
5V
7
GND

6


5V
20mS
50uS
tww
CK
GND
BIT
NO
PROG
5V
1037mS
GND

7


5V
20mS
CK
GND
E3
5V
9
GND

8

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

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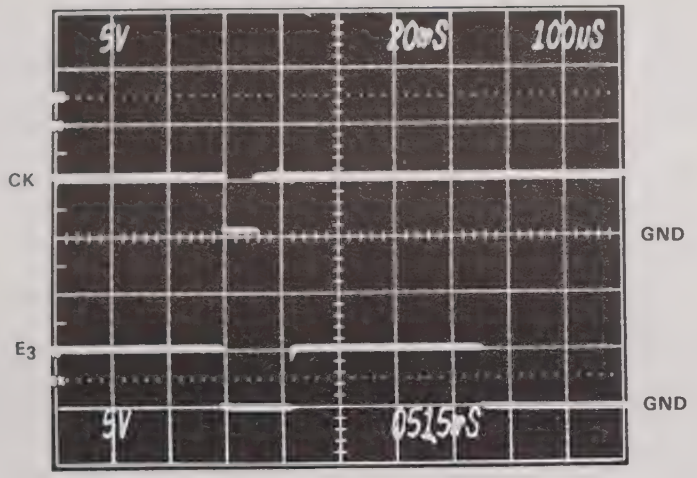
TIMING DIAGRAM

FAMILY CODES 51, 52

DATA I/O

0526/1282



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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

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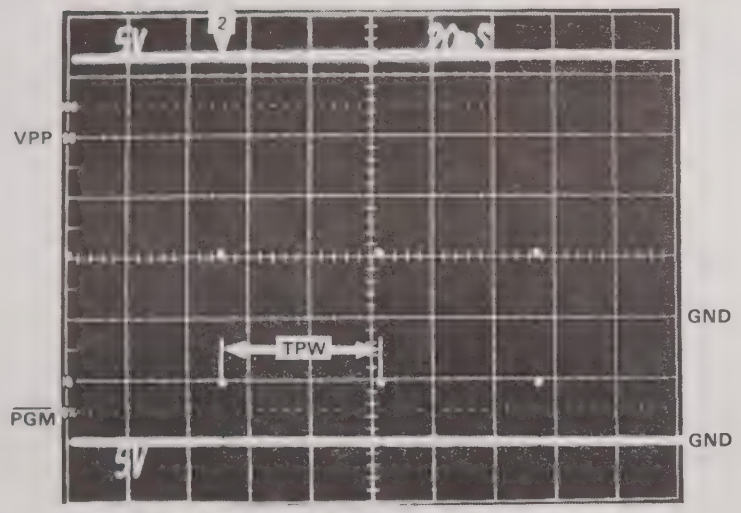
TIMING DIAGRAM

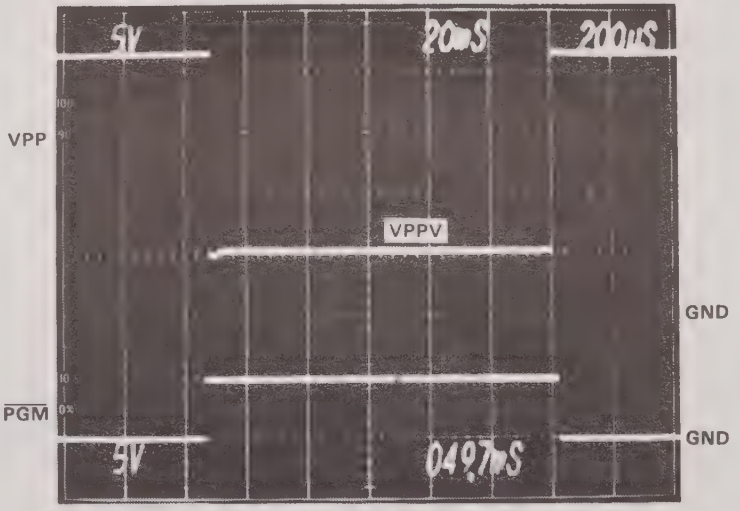
FAMILY CODES 51, 52

DATA I/O

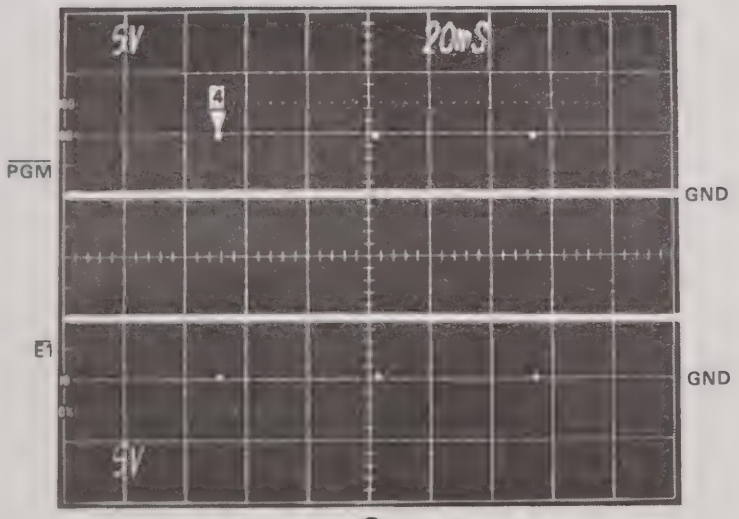
0526/1282


5V
20mS
VPP
TPW
GND
PGM
GND
5V

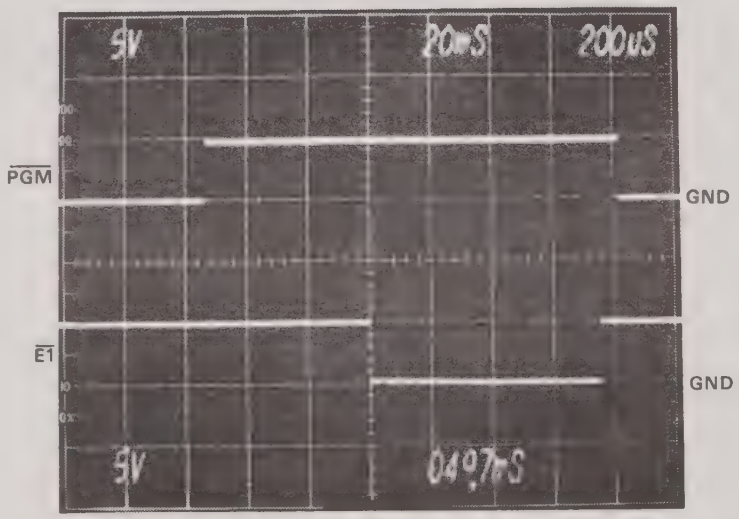
1


5V
20mS
200uS
VPP
VPPV
GND
PGM
GND
5V
049.7mS

2


5V
20mS
PGM
GND
E1
GND
5V

3


5V
20mS
200uS
PGM
GND
E1
GND
5V
049.7mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 53.*
2. *Load RAM with hex 01 for Family 54 and bit-to-prog waveform becomes bit-no-prog waveform.*

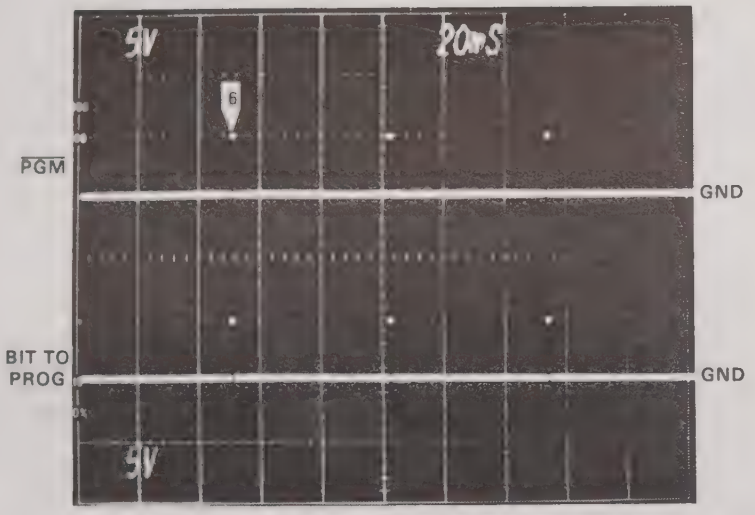
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	C73	3/84

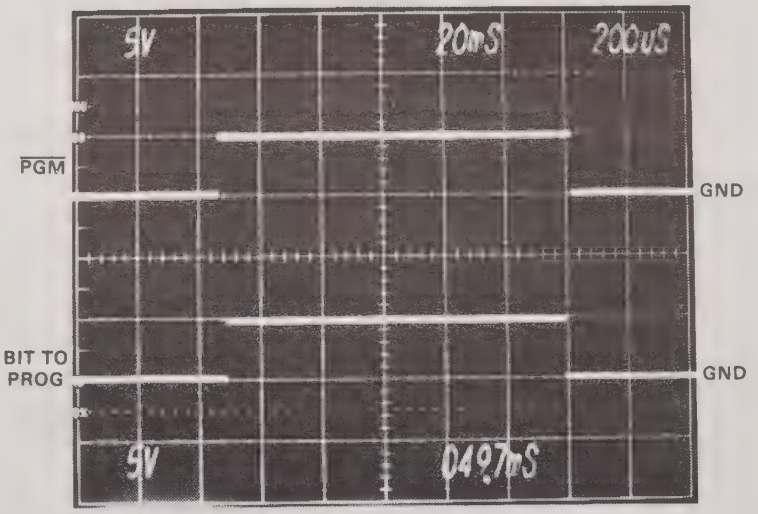
TIMING DIAGRAM

FAMILY CODES 53, 54

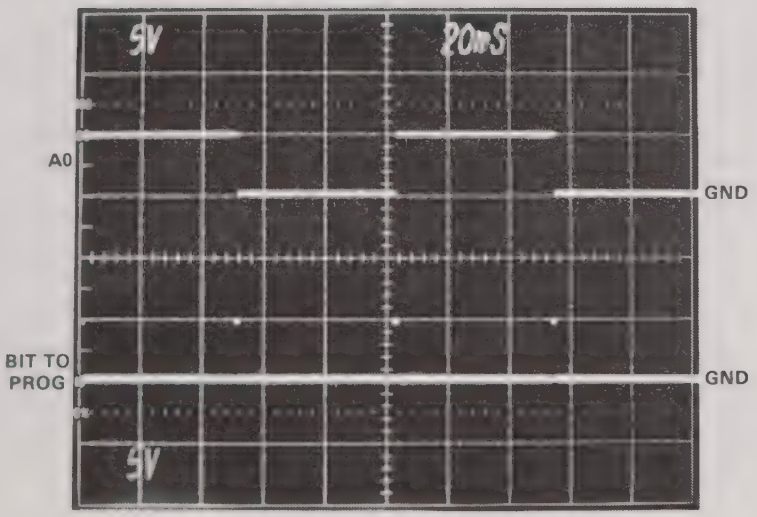
DATA I/O


5V
20mS
6
PGM
GND
BIT TO PROG
GND
5V

5


5V
20mS
200uS
PGM
GND
BIT TO PROG
GND
5V
049?mS

6


5V
20mS
A0
GND
BIT TO PROG
GND
5V

7

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

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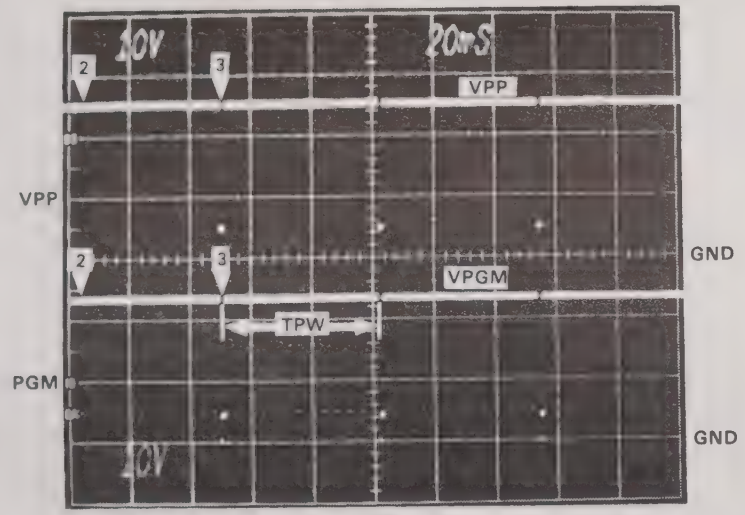
TIMING DIAGRAM

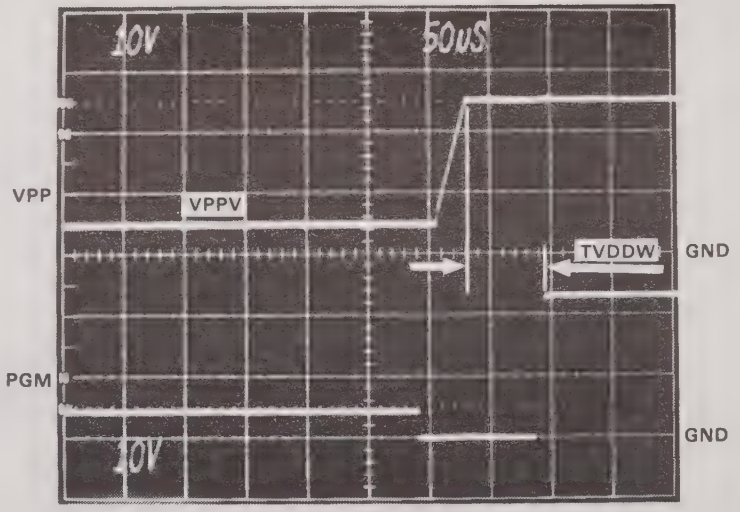
FAMILY CODES 53, 54

DATA I/O

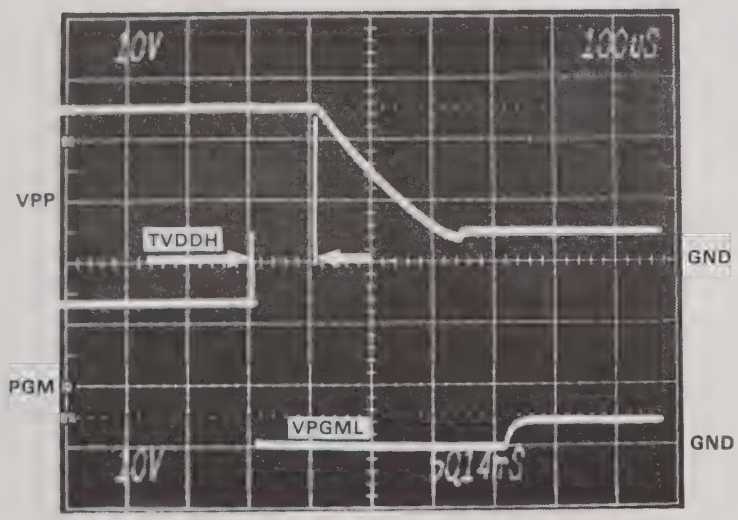
0526/1282


10V
20mS
2
3
VPP
VPP
GND
VPGM
TPW
PGM
GND
10V

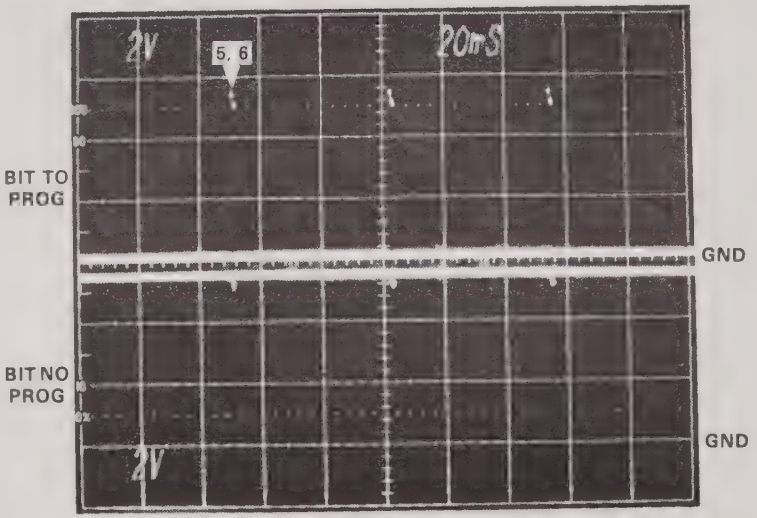
1


10V
50uS
VPP
VPPV
TVDDW
GND
PGM
GND
10V

2


10V
100uS
VPP
TVDDH
GND
PGM
VPGML
GND
10V
50.14mS

3


2V
5, 6
20mS
BIT TO PROG
GND
BIT NO PROG
GND
2V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.9	5.0	5.1	V	Not shown
	VEA	21.5	23.0	24.5	V	Not shown
	VPP	24.0	25.0	26.0	V	
	VPPV	4.0	5.0	5.2	V	
	VPGM	21.5	23.0	24.5	V	
	VPGML		0	0.3	V	
	TVDDW	17			µs	See note 3
	TVDDH	0			µs	See note 3
	TPW	50		60	ms	
	TWW	17			µs	See note 3
	TAW	17			µs	See note 3
	TWA	17			µs	See note 3
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4 9	V	
	VREF	0.6	0 7	0 8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5 1	5 2	5 3	V	
	VREF	2.1	2.2	2 3	V	701-1998/TP4
	High Load	0	0	0 4	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 55.*
2. *Load Ram with hex 01 for Family 56 and bit-to-prog waveform becomes bit-no-prog waveform and vice versa.*
3. *4TCY = 17 µs @ 3.579545 MHz.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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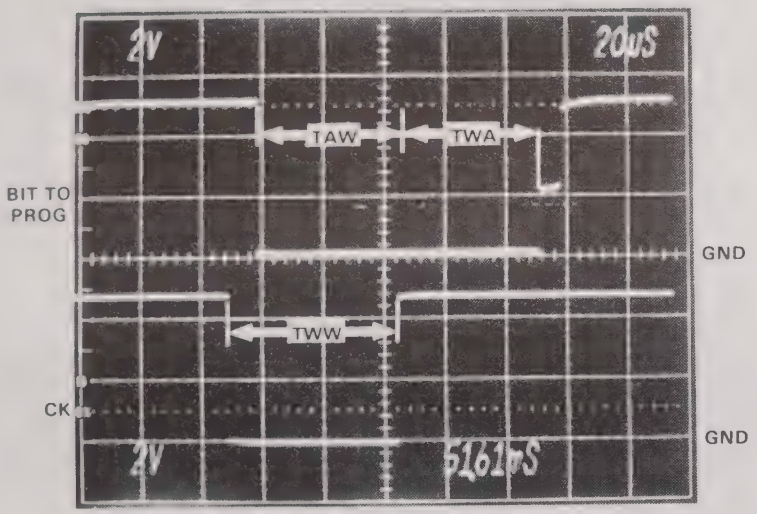
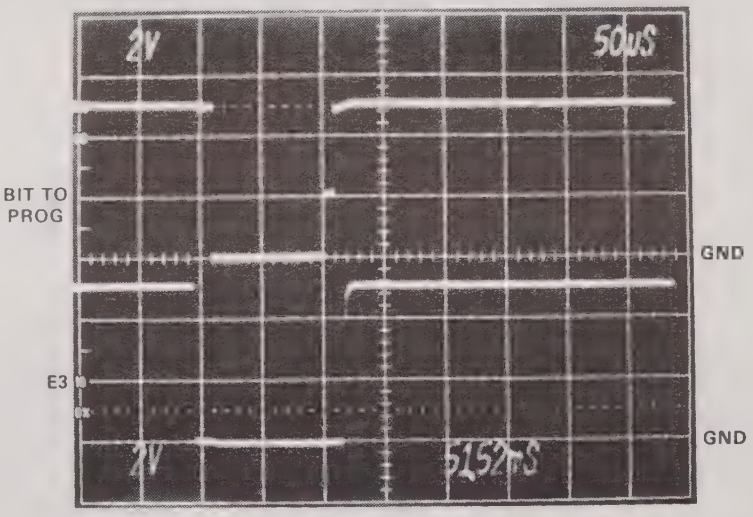
TIMING DIAGRAM

FAMILY CODES 55, 56

DATA I/O


2V
20uS
TAW
TWA
BIT TO PROG
GND
TWW
CK
GND
2V
5161mS

5


2V
50uS
BIT TO PROG
GND
E3
GND
2V
5152mS

6

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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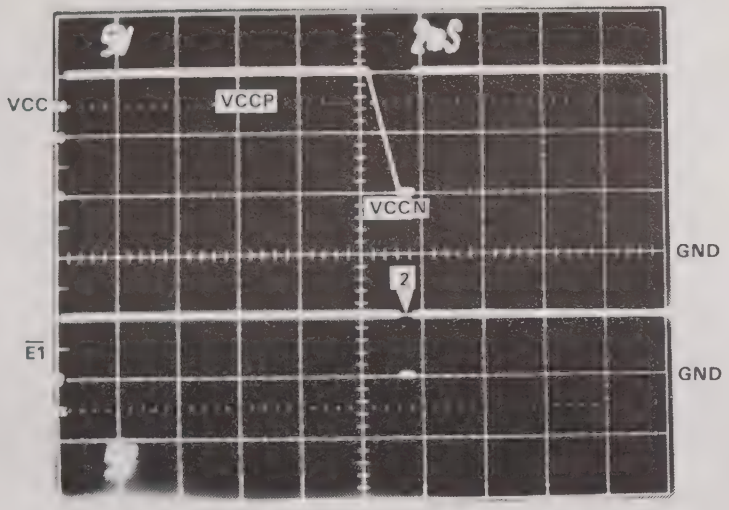
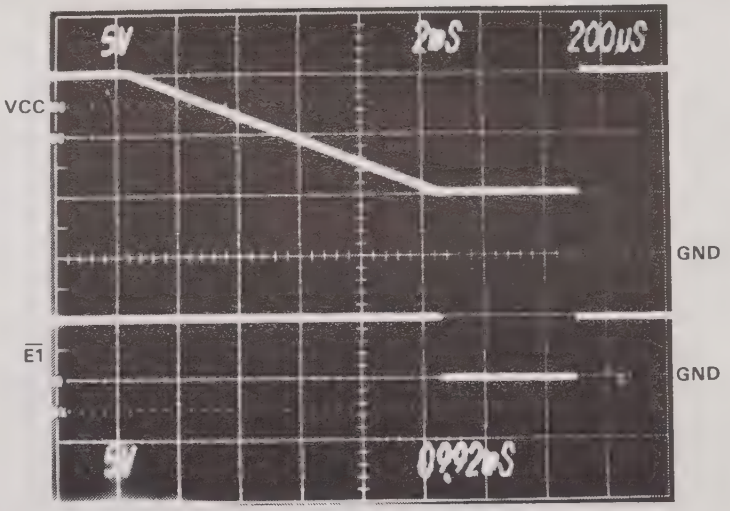
TIMING DIAGRAM

FAMILY CODES 55, 56

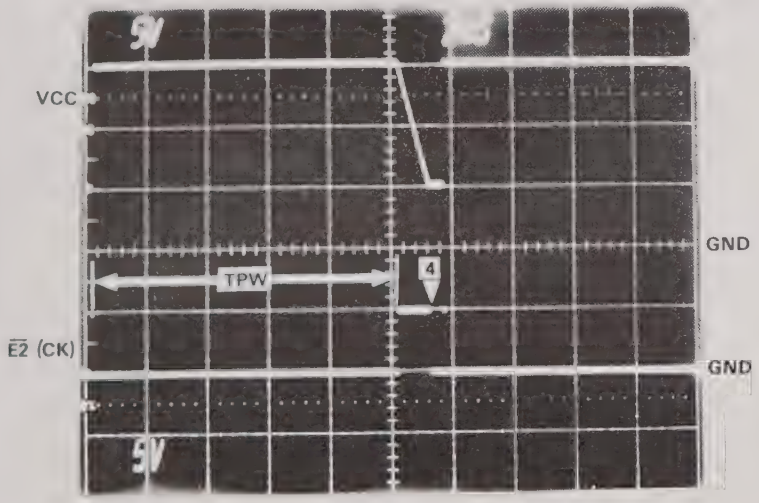
DATA I/O


5V
2mS
VCC
VCCP
VCCN
GND
2
$\overline{E1}$
GND
5V

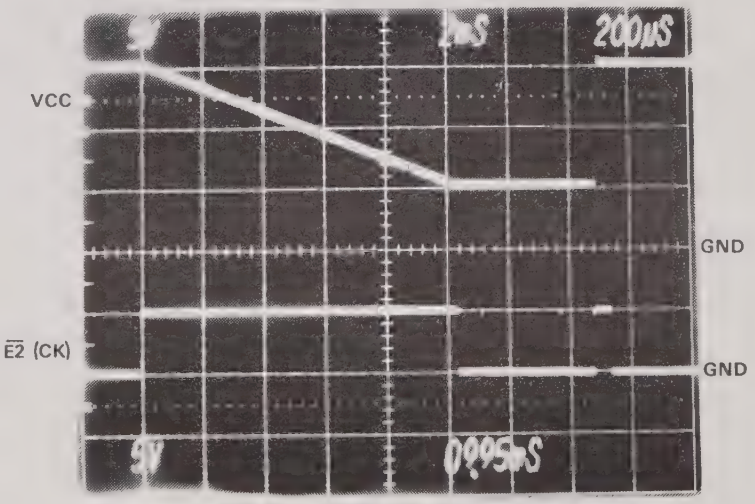
1


5V
2mS
200uS
VCC
GND
$\overline{E1}$
GND
5V
0.992mS

2


5V
VCC
GND
TPW
4
$\overline{E2}$ (CK)
GND
5V

3


5V
2mS
200uS
VCC
GND
$\overline{E2}$ (CK)
GND
5V
0.995mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	14.0	15.0	16.0	V	
	VCCN	4.0	5.0	6.0	V	
	TPW	9.8	10.0	10.2	ms	
	TR					NA
	TF					NA
	Reject		2		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.4	V	701-1998/TP2
	Low Load	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 57, and bit-no-prog waveform becomes bit-to-prog waveform.*
2. *Load RAM with hex 01 for Family 58.*
3. *Photos 7 and 8 are erase waveforms.*
4. *On the E2(CK) pin, one or two clock pulses may be seen, depending on which pulse location is observed.*
5. *Photo 5 is for Family 58. For Family 57, it is bit-to-prog.*

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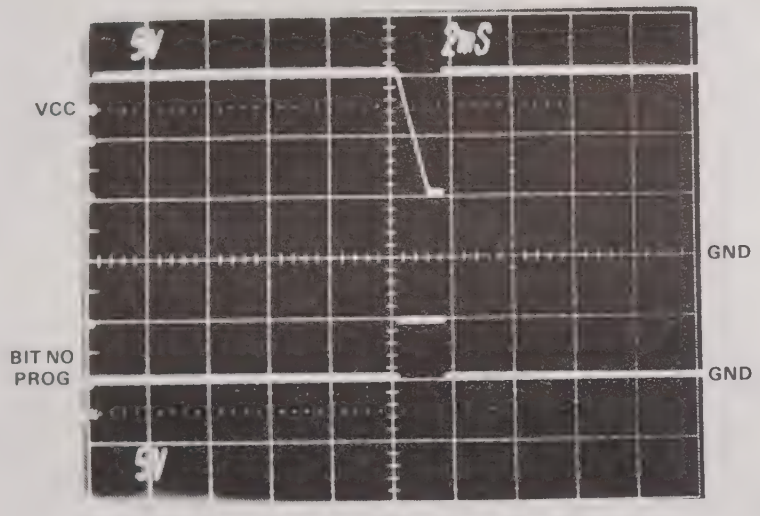
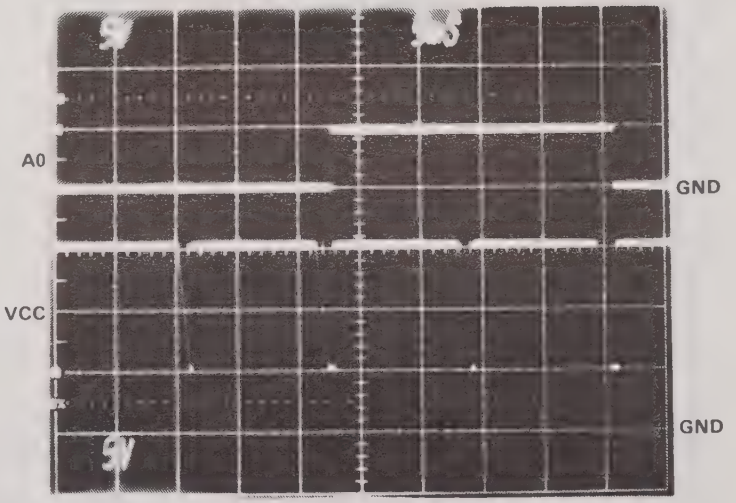
TIMING DIAGRAM

FAMILY CODES 57, 58

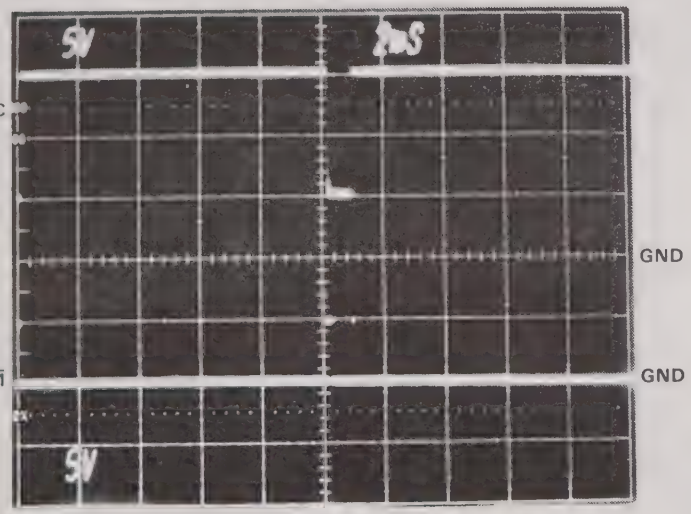
DATA I/O


5V
2mS
VCC
GND
BIT NO
PROG
GND
5V

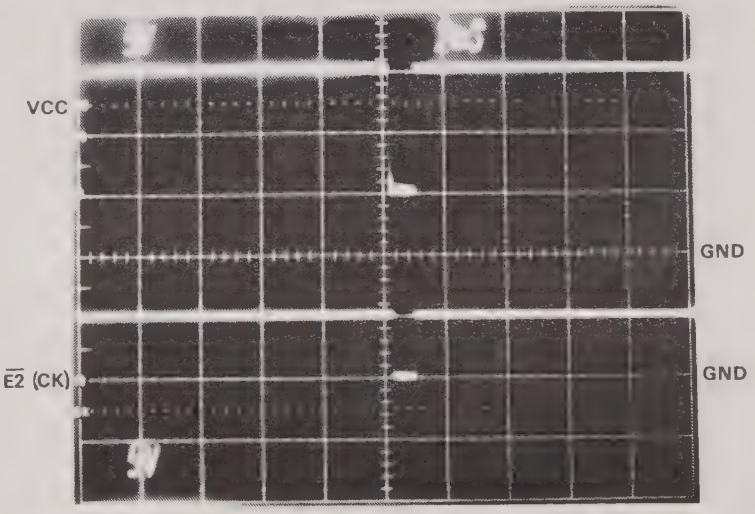
5


5V
2mS
A0
GND
VCC
GND
5V

6


5V
2mS
VCC
GND
$\overline{E1}$
GND
5V

7


5V
2mS
VCC
GND
$\overline{E2}$ (CK)
GND
5V

8

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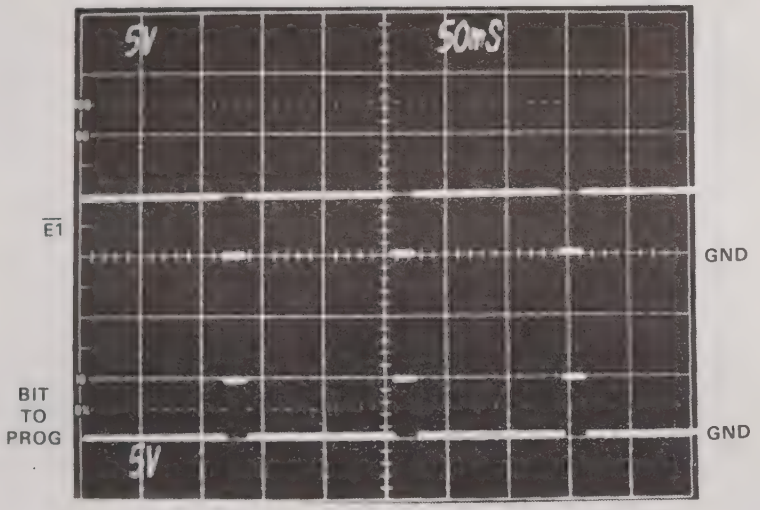
TIMING DIAGRAM

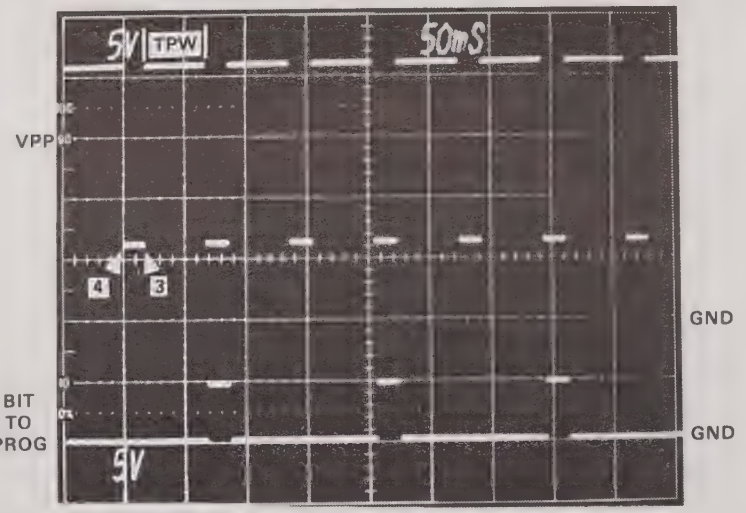
FAMILY CODES 57, 58

DATA I/O

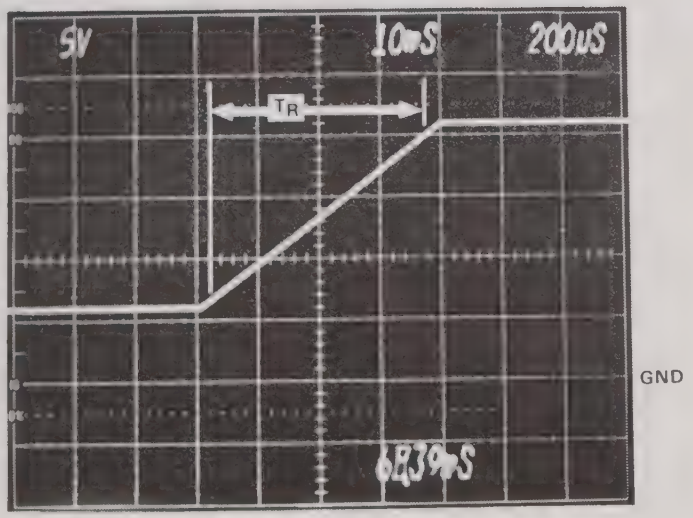
0526/1282


5V
50mS
$\overline{E1}$
GND
BIT
TO
PROG
GND
5V

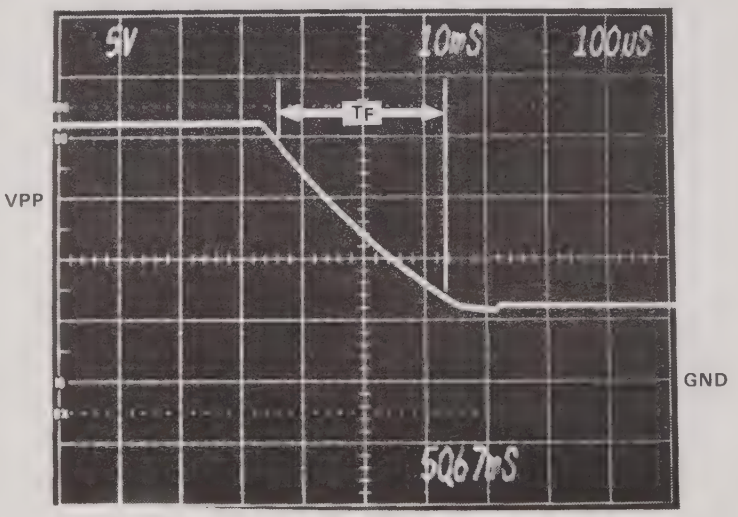
1


5V
TPW
50mS
VPP
4
3
GND
BIT
TO
PROG
GND
5V

2


5V
10mS
200uS
TR
VPP
GND
6.839mS

3


5V
10mS
100uS
TF
VPP
GND
5.067mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.5	5.8	6.1	V	Not Shown
	VPP	20.0	20.5	21.0	V	
	VPPN	5.7	5.9	6.1	V	
	TPW	45	50	55	ms	
	T_R	50			µs	
	T_F	50			µs	
	Reject		4		Pulses	See note 3
	Overprogram		1		Pulses	See note 3
1ST PASS VERIFY	V_{CC}	4.8	4.9	5.0	V	
	V_{REF}	0.7	0.8	0.9	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	16.5	17.5	18.5	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	3.4	3.5	3.6	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	19.2	20.2	21.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 59.*
2. *Load RAM with hex 01 for Family 60, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Pulse 2 of the 4-pulse string is actually an overprogram pulse.*

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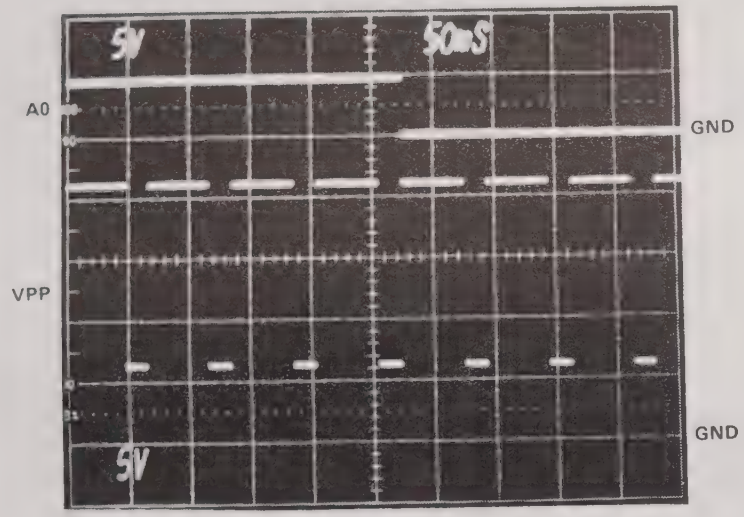
TIMING DIAGRAM

FAMILY CODES 59, 60

DATA I/O



5

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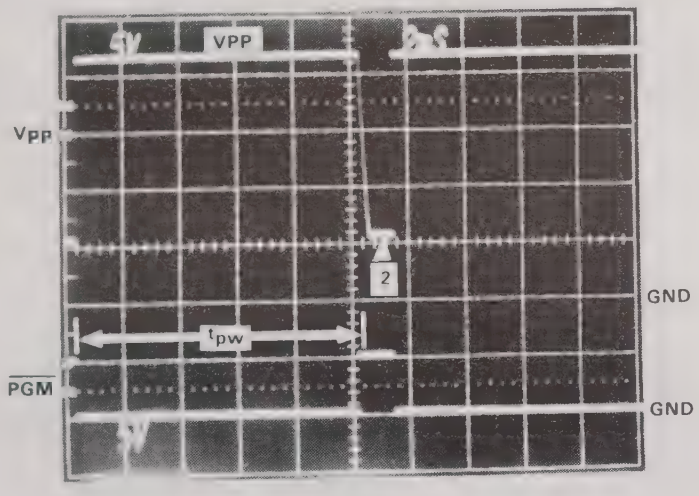
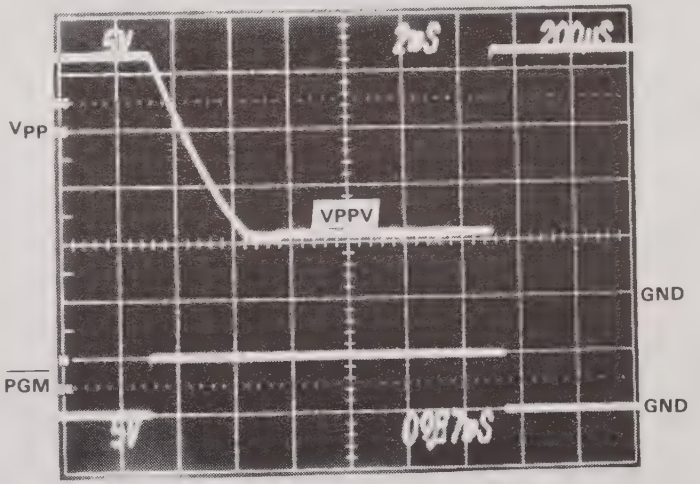
TIMING DIAGRAM

FAMILY CODES 59, 60

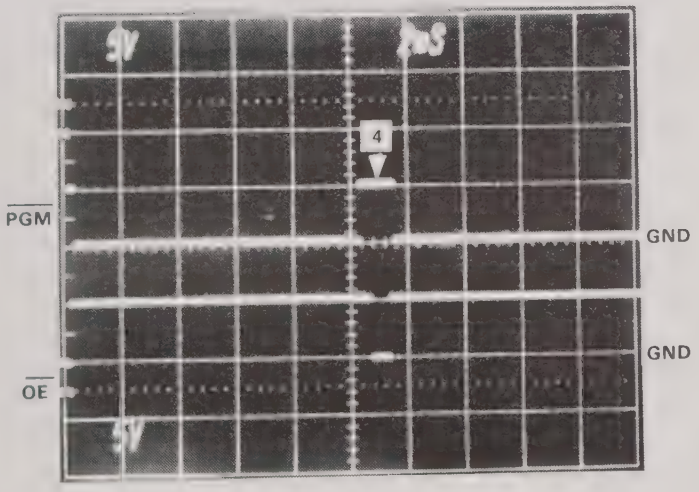
DATA I/O


5V
VPP
2mS
VPP
2
GND
tpw
PGM
GND
5V

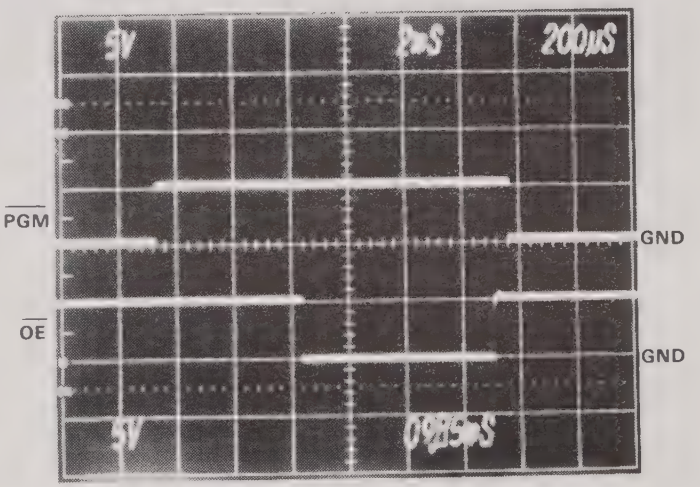
1


5V
2mS
200uS
VPP
VPPV
GND
PGM
GND
5V

2


5V
2mS
4
PGM
GND
GND
OE
5V

3


5V
2mS
200uS
PGM
GND
OE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	20.5	21.0	21.5	V	
	V_{PPV}	4.75	5.0	5.25	V	
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 63.*
2. *Photos 7 and 8 are for Pinout 24.*

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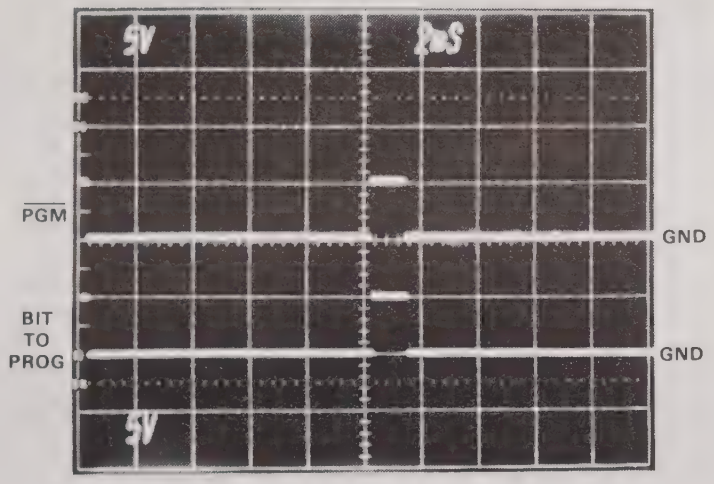
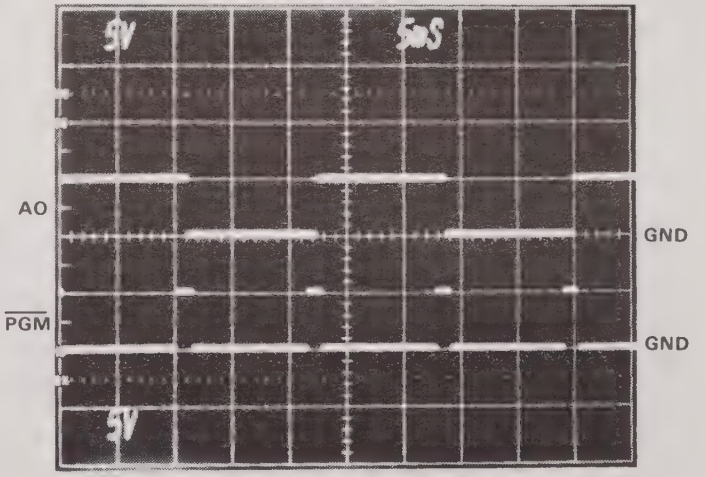
TIMING DIAGRAM

FAMILY CODES 63, 64

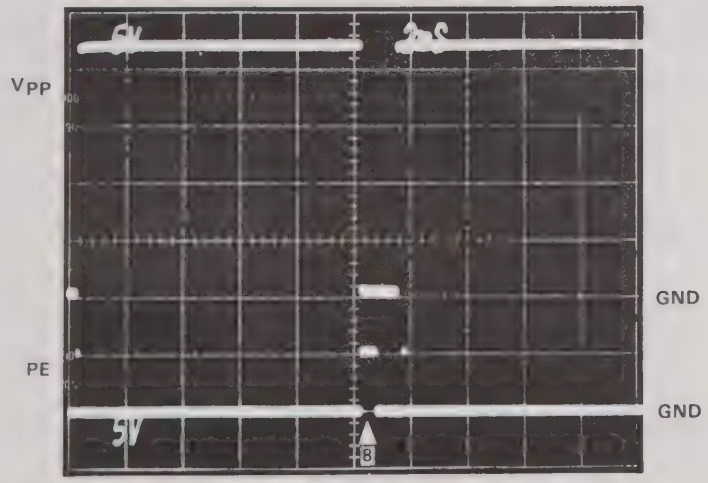
DATA I/O


5V
2mS
PGM
GND
BIT
TO
PROG
GND
5V

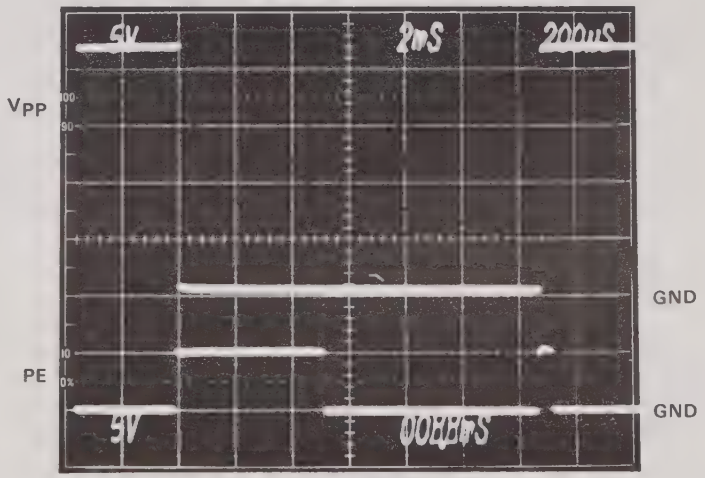
5


5V
5mS
AO
GND
PGM
GND
5V

6


5V
2mS
VPP
GND
PE
GND
5V
8

7


5V
2mS
200uS
VPP
GND
PE
GND
5V

8

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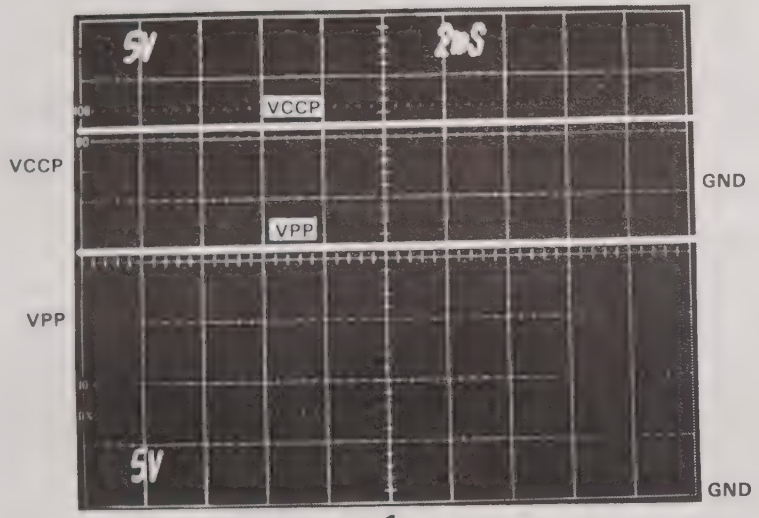
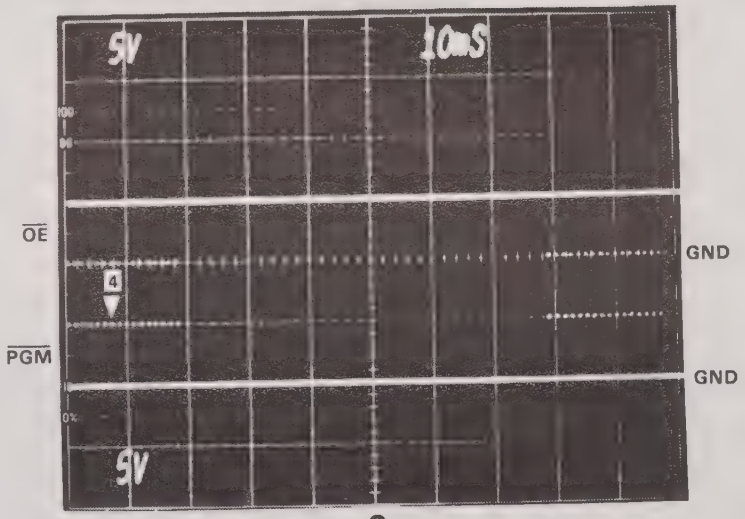
TIMING DIAGRAM

FAMILY CODES 63, 64

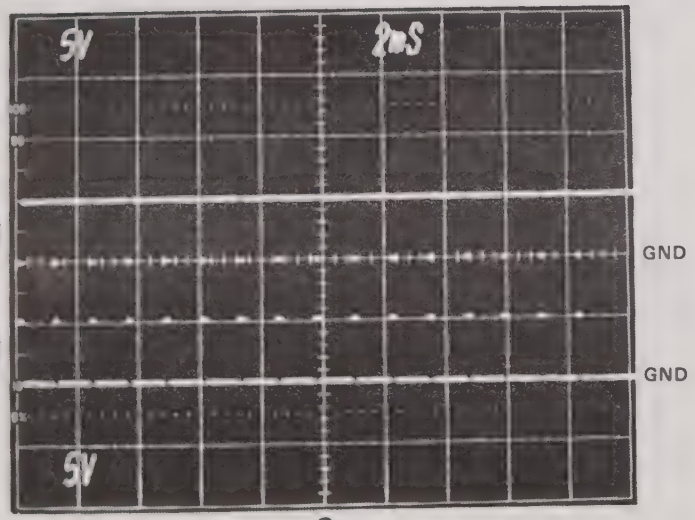
DATA I/O


5V
2mS
VCCP
VPP
5V
VCCP
VPP
GND
GND

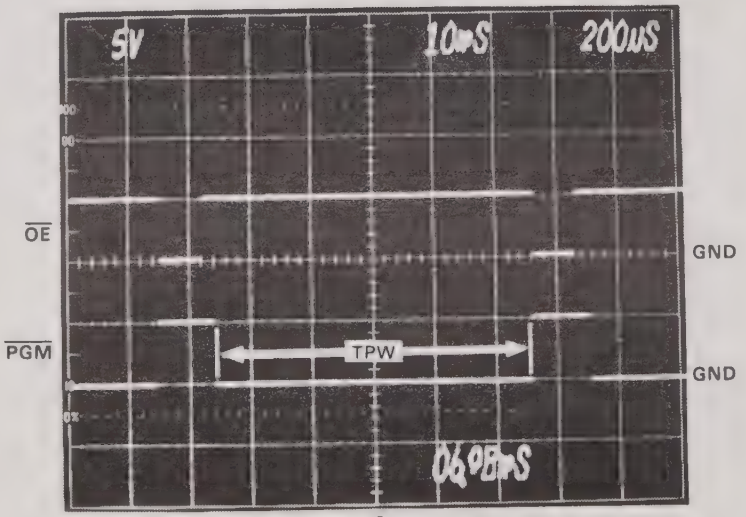
1


5V
10mS
OE
PGM
4
5V
GND
GND

2


5V
2mS
OE
PGM
5V
GND
GND

3


5V
10mS
200uS
OE
PGM
TPW
GND
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV					NA
	TPW	0.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		15		Pulses	
	Overprogram		1		Pulses	See Note 3
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 79.*
2. *Load RAM with hex 01 for Family 80, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse follows the reject pulses and its length is the number of reject pulses multiplied by 4 ms.*

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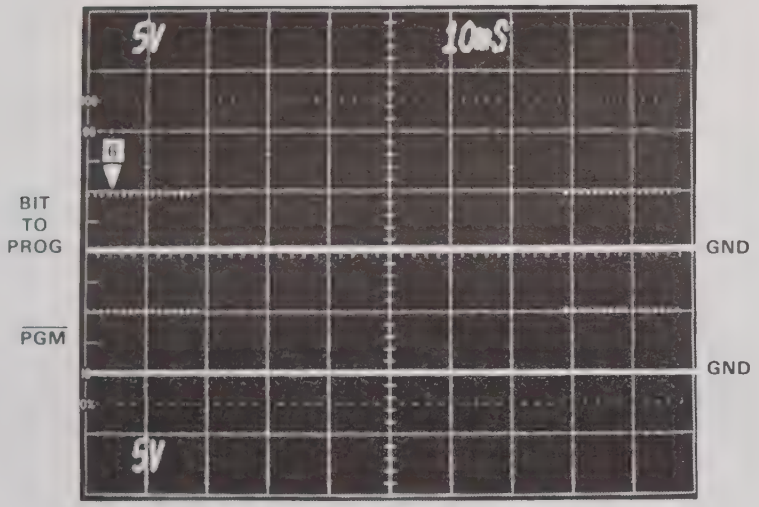
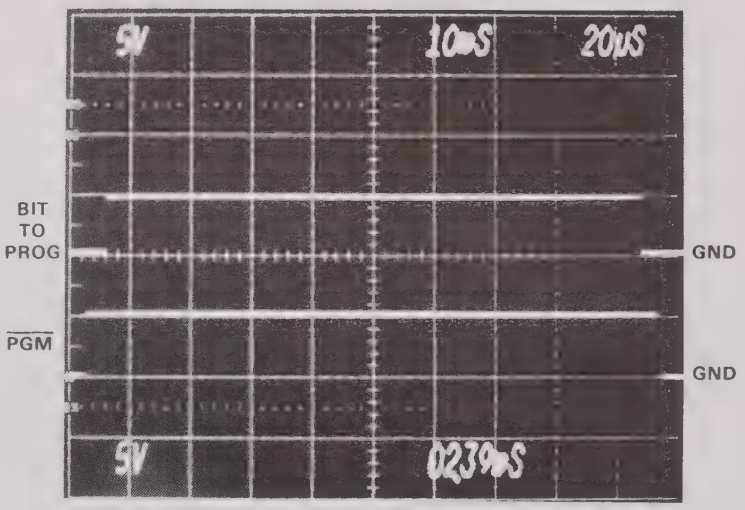
TIMING DIAGRAM

FAMILY CODES 79, 80

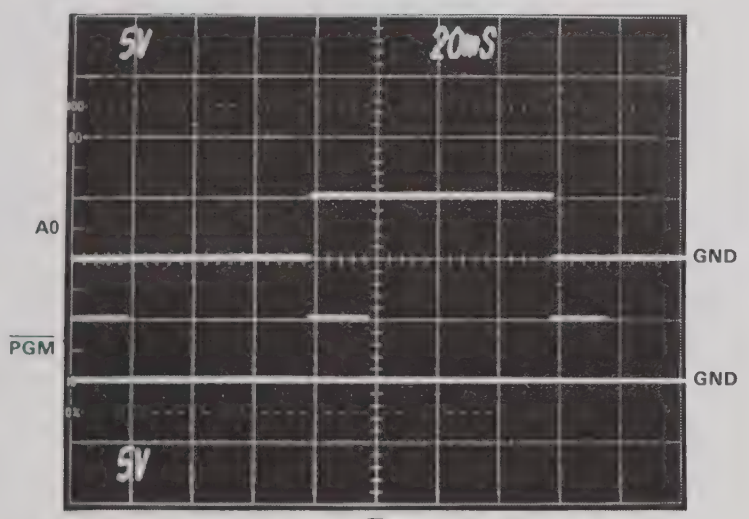
DATA I/O


5V
10mS
BIT
TO
PROG
GND
PGM
GND
5V

5


5V
10mS
20µS
BIT
TO
PROG
GND
PGM
GND
5V
0239mS

6


5V
20mS
A0
GND
PGM
GND
5V

7

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TIMING DIAGRAM

FAMILY CODES 79, 80

DATA I/O

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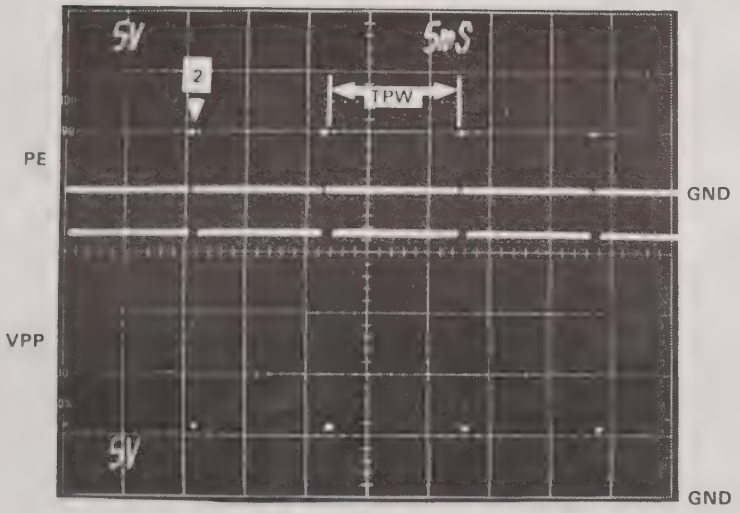
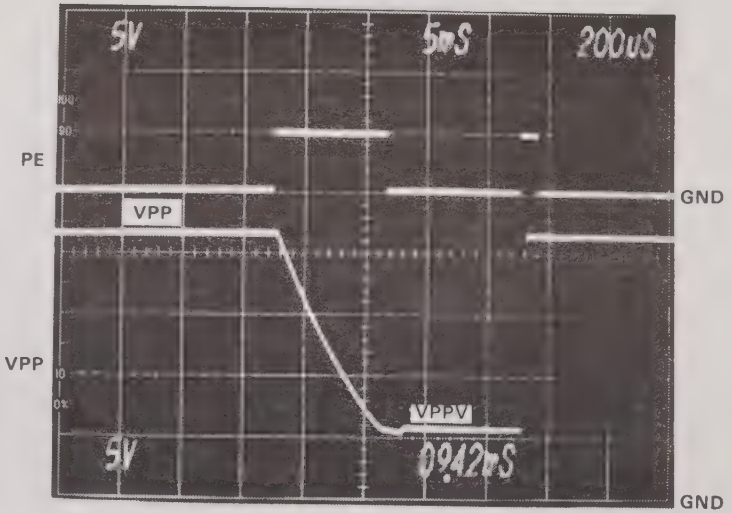
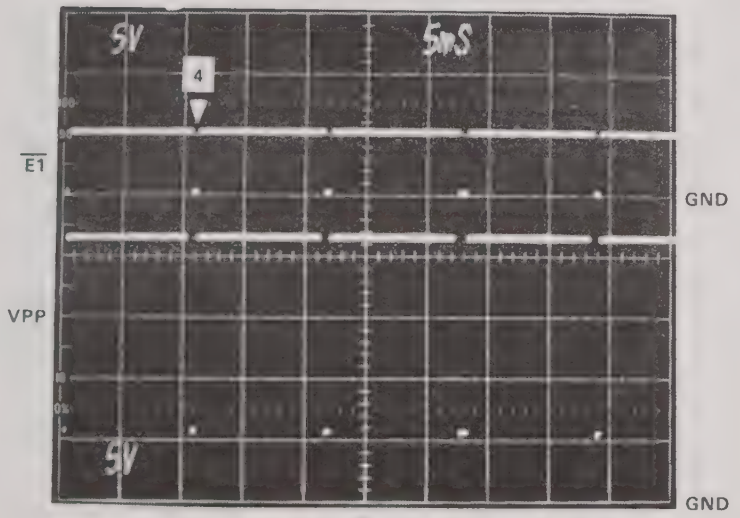

5V
5mS
2
TPW
PE
GND
VPP
5V
GND

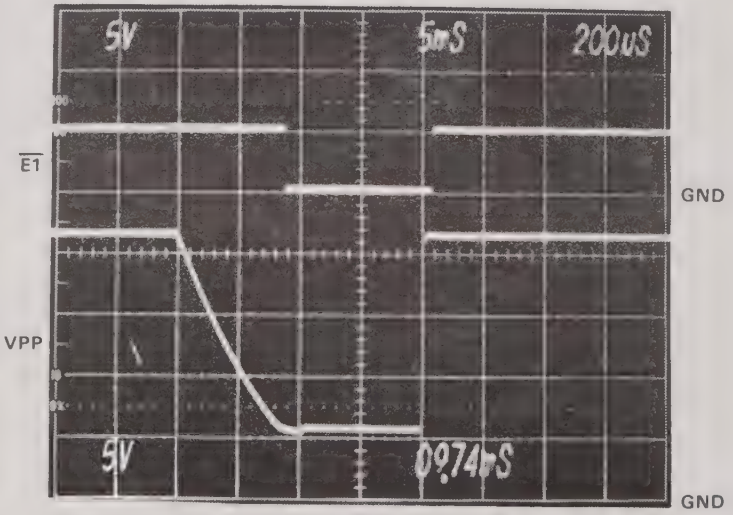
1


5V
5mS
200uS
PE
GND
VPP
VPP
VPPV
5V
09.42mS
GND

2


5V
5mS
4
E1
GND
VPP
5V
GND

3


5V
5mS
200uS
E1
GND
VPP
5V
09.74mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	9.8	10.0	10.2	ms	
	TR	1			µs	
	TF	1			µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 81.*
2. *Load RAM with hex 01 for Family 82, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photos 13 through 18 are Byte erase waveforms.*

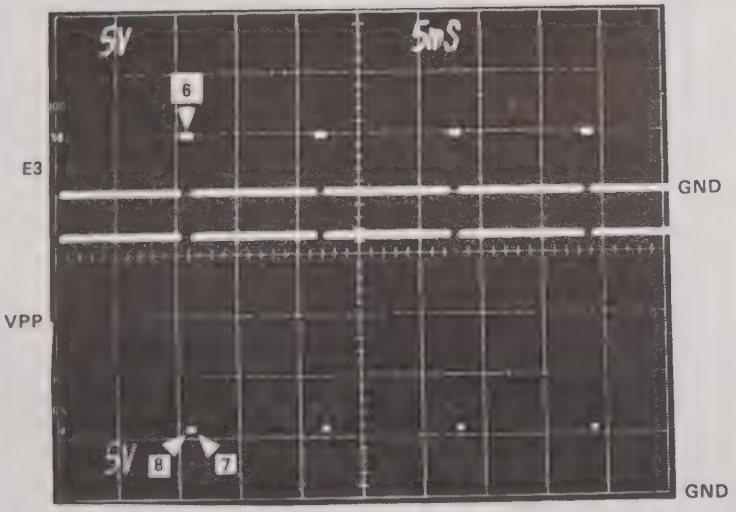
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

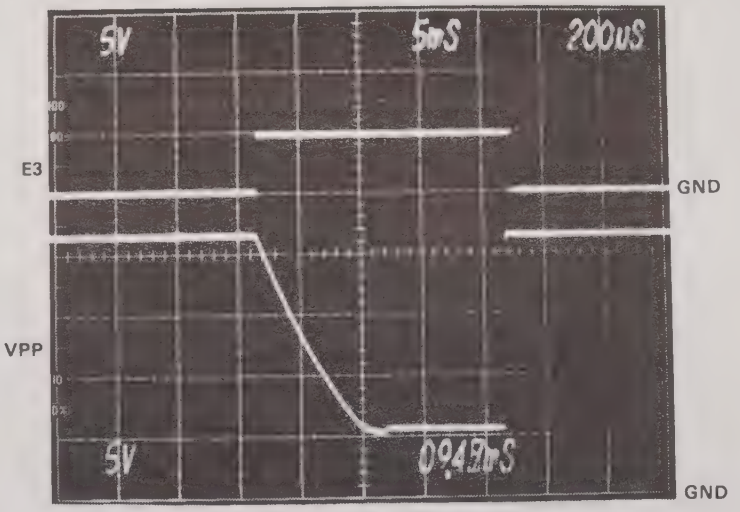
TIMING DIAGRAM

FAMILY CODES 81, 82

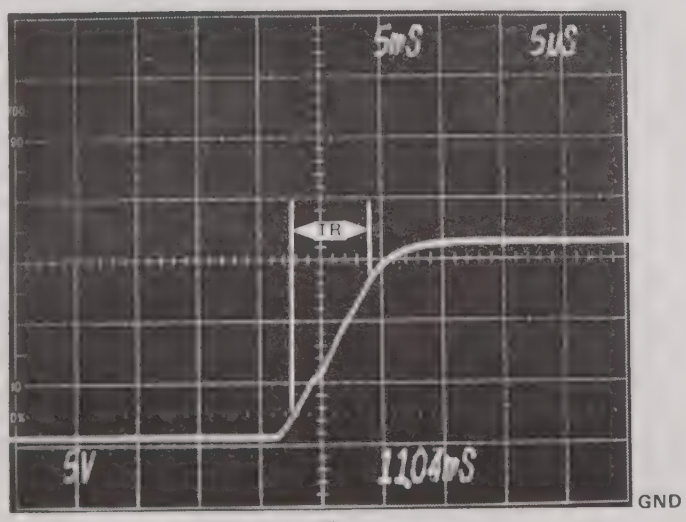
DATA I/O


5V
5mS
6
E3
GND
VPP
5V
8
7
GND

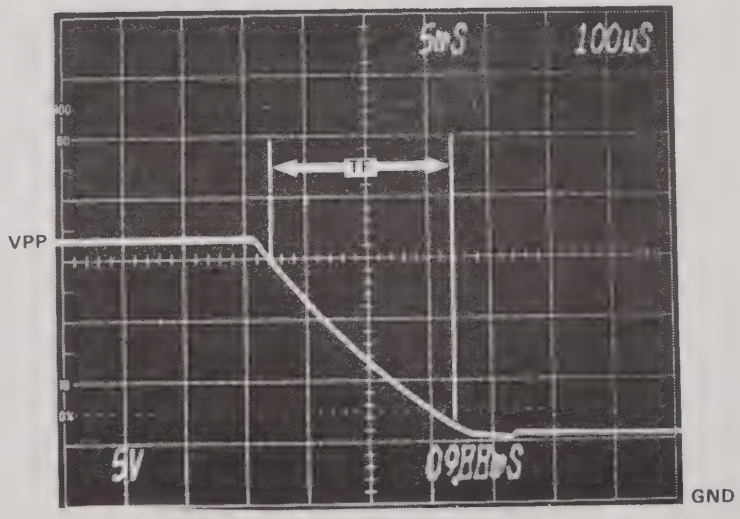
5


5V
5mS
200uS
E3
GND
VPP
5V
GND

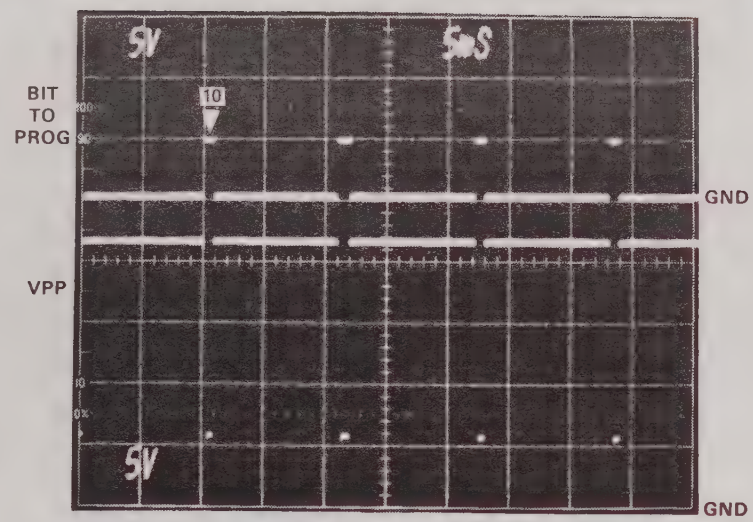
6


5mS
5uS
TR
VPP
5V
1104mS
GND

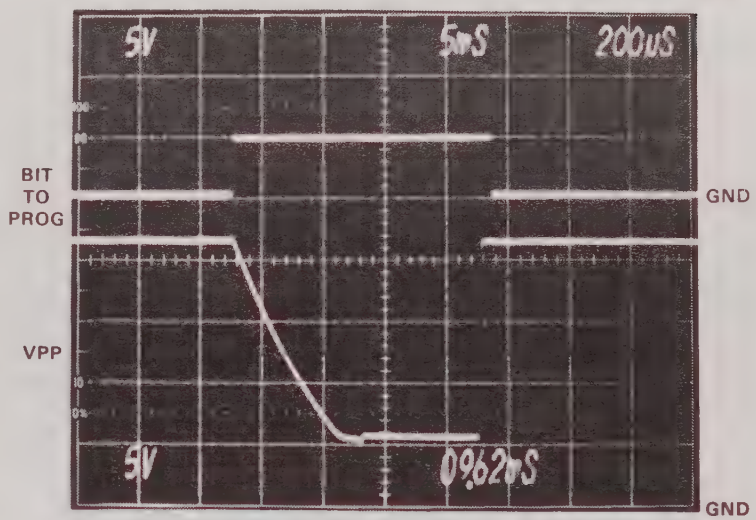
7


5mS
100uS
TF
VPP
5V
GND

8



9



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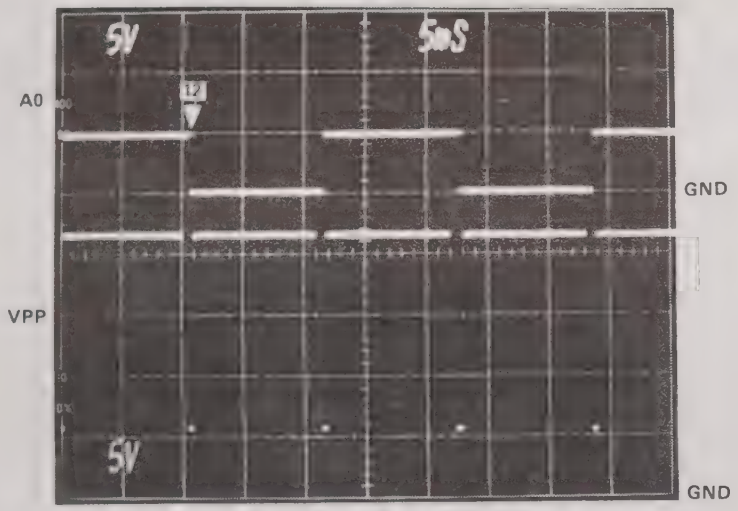
	ECN #5022	CTJ	3/84

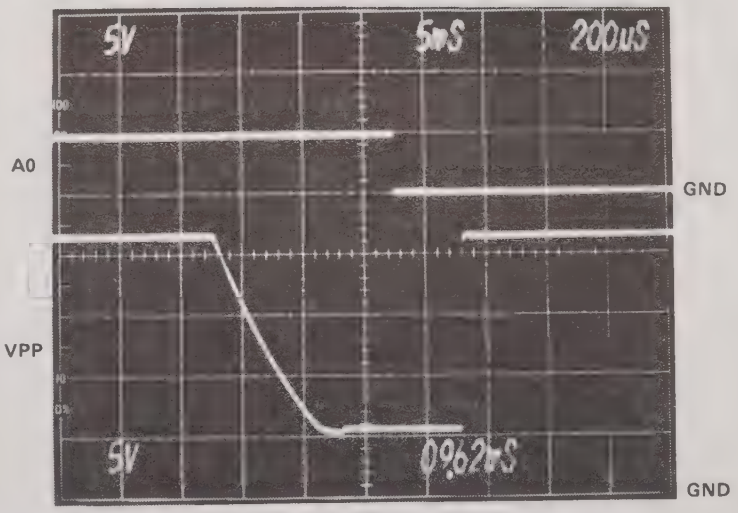
TIMING DIAGRAM

FAMILY CODES 81, 82

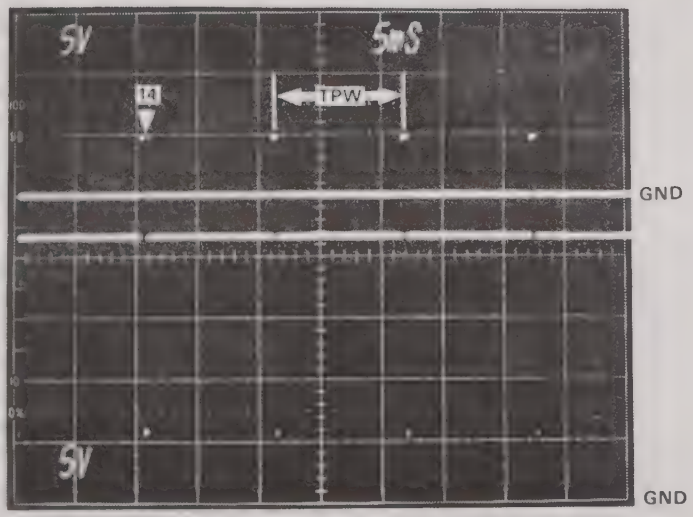
DATA I/O


5V
5mS
A0
12
GND
VPP
5V
GND

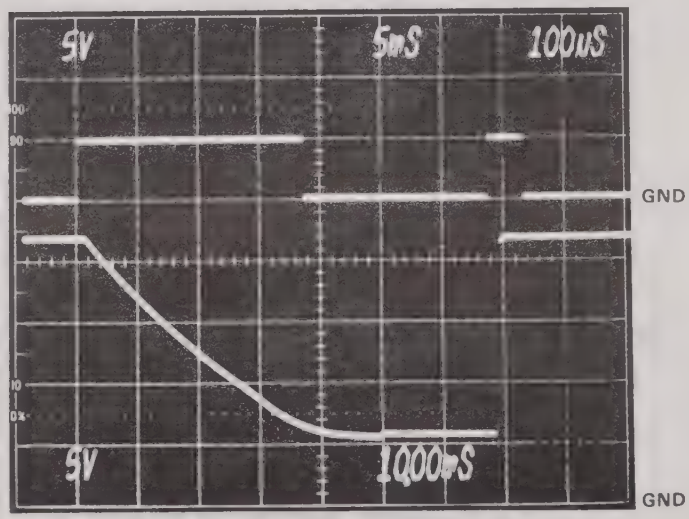
11


5V
5mS
200uS
A0
GND
VPP
5V
0%2mS
GND

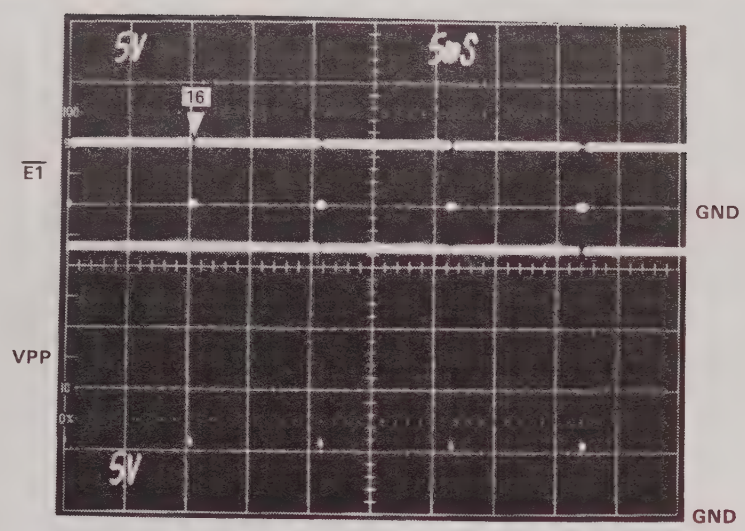
12


5V
5mS
14
TPW
PE
GND
VPP
5V
GND

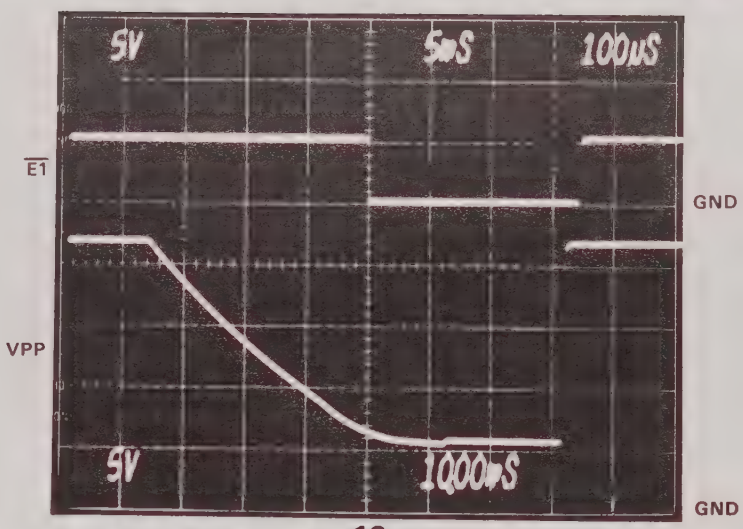
13


5V
5mS
100uS
PE
GND
VPP
5V
1000mS
GND

14



15



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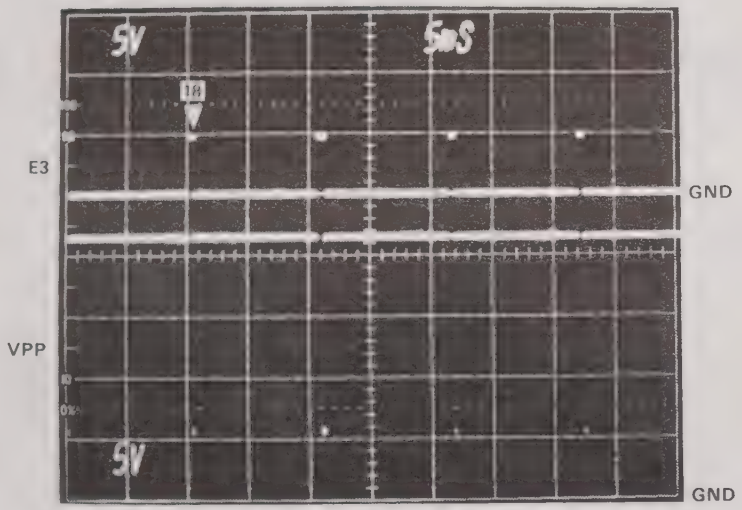
TIMING DIAGRAM

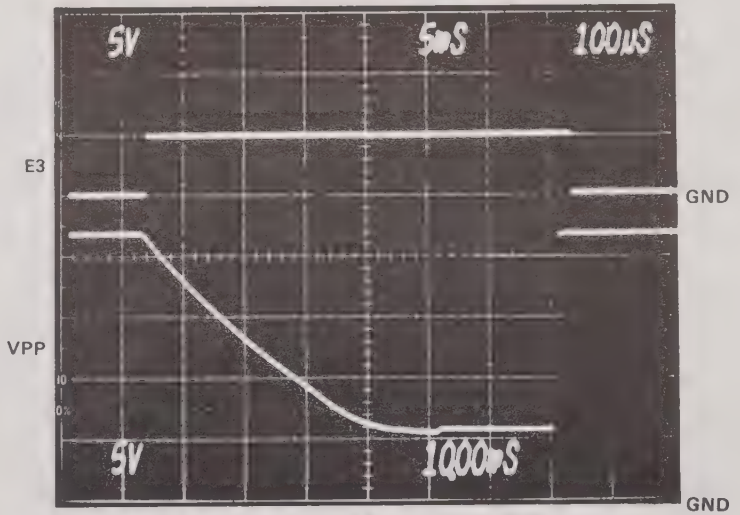
FAMILY CODES 81, 82

DATA I/O

0526-1282



17



18

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	ECN #5022	CTJ	3/84

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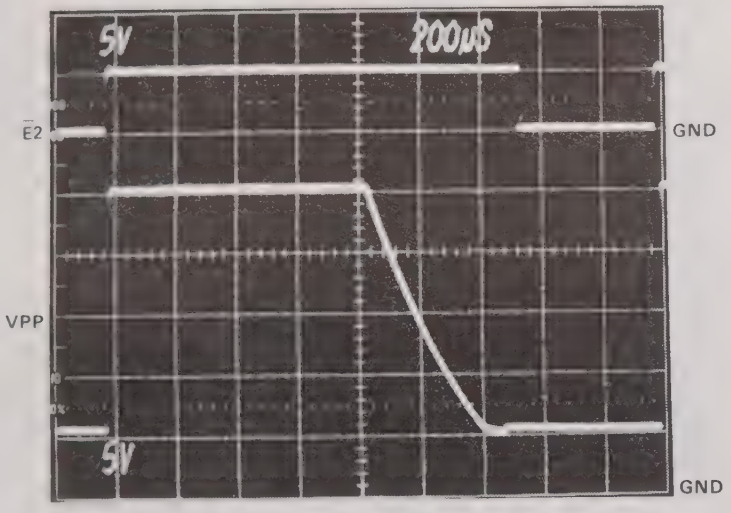
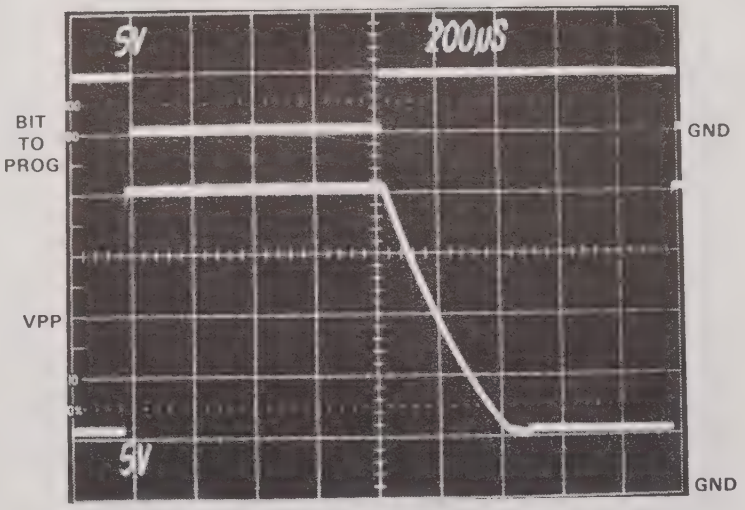
TIMING DIAGRAM

FAMILY CODES 81, 82

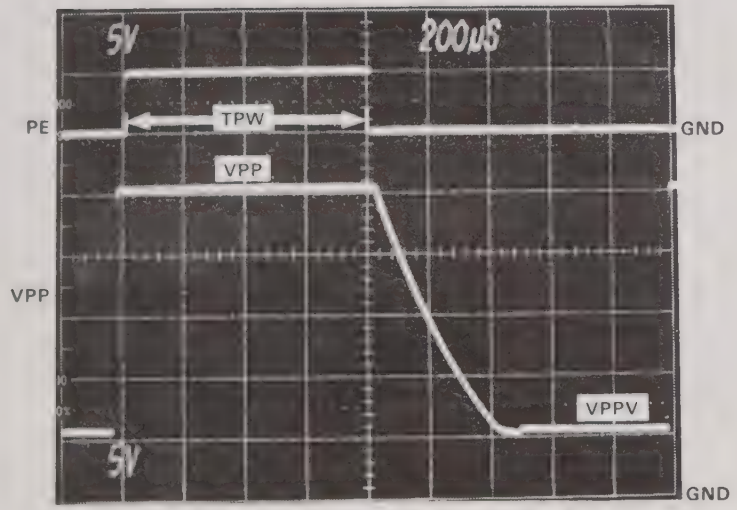
DATA I/O


5V
200µS
E2
GND
VPP
5V
GND

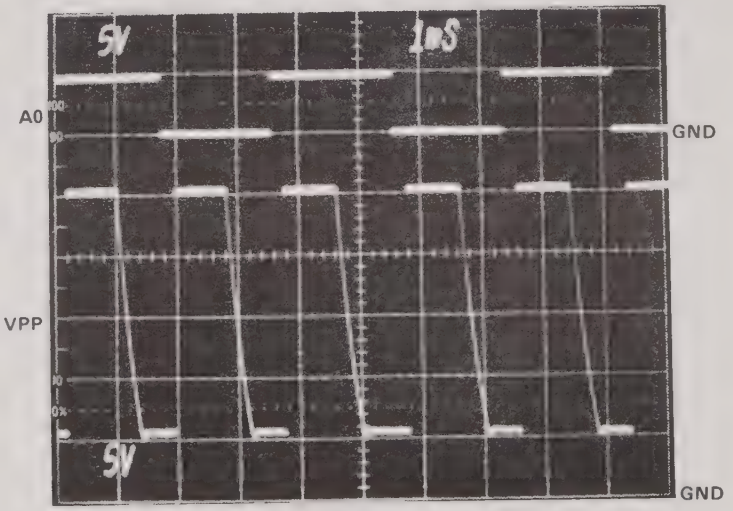
1


5V
200µS
BIT
TO
PROG
GND
VPP
5V
GND

2


5V
200µS
PE
TPW
GND
VPP
VPP
VPPV
5V
GND

3


5V
1mS
A0
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	800			µs	
	TR	5			ns	
	TEP	1			sec	
	TF	5			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 83.*
2. *Load RAM with hex 01 for Family 84, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photo 7 is the erase waveform.*

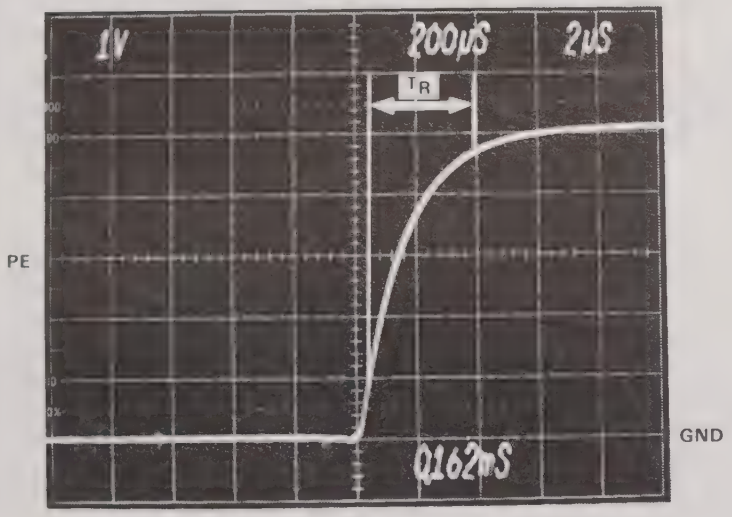
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

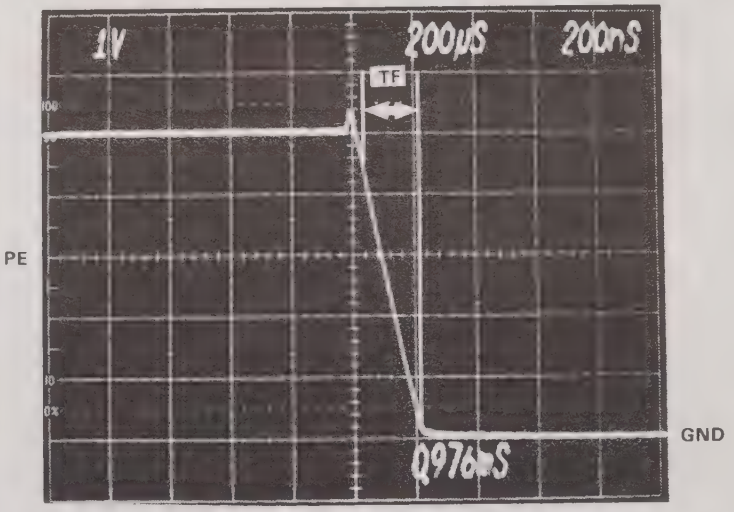
TIMING DIAGRAM

FAMILY CODES 83, 84

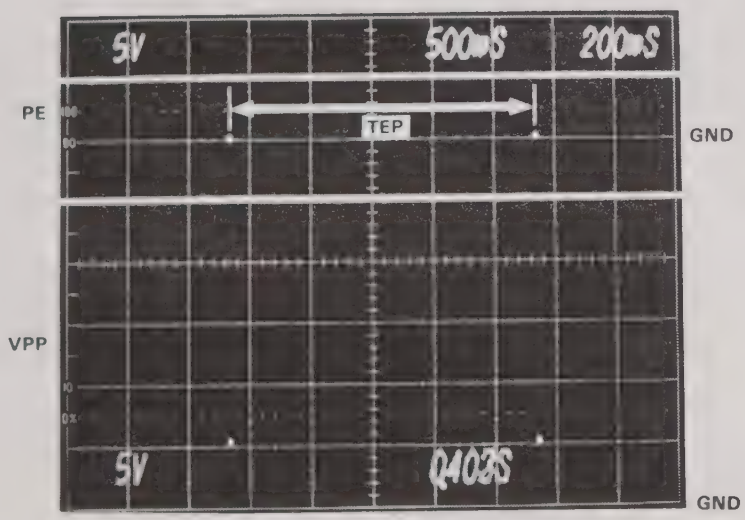
DATA I/O


1V
200µS
2µS
TR
PE
GND

5


1V
200µS
200nS
TF
PE
GND

6


5V
500mS
200mS
TEP
PE
GND
VPP
5V
GND

7

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	ECN #5022	CTZ	3/84

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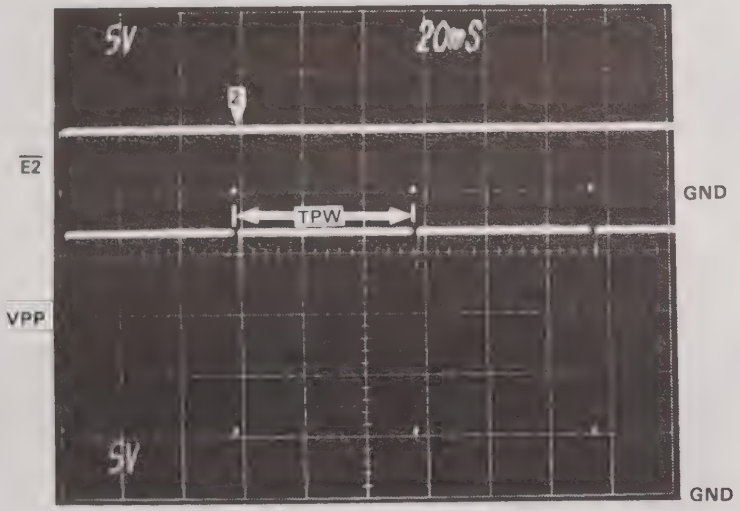
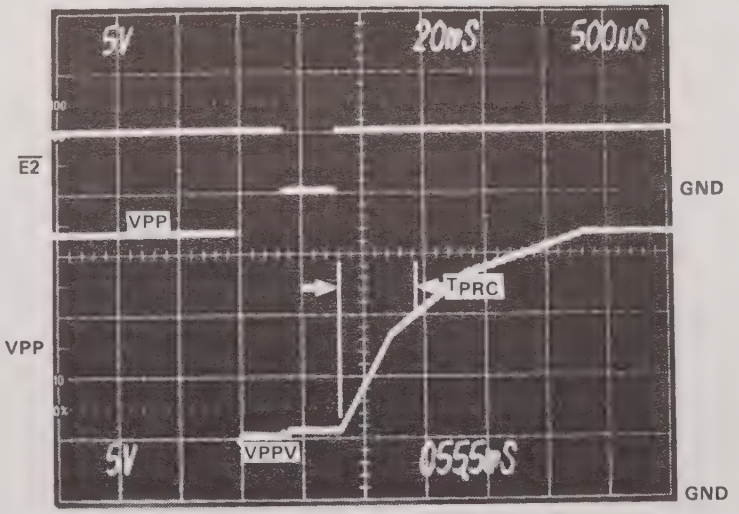
TIMING DIAGRAM

FAMILY CODES 83, 84

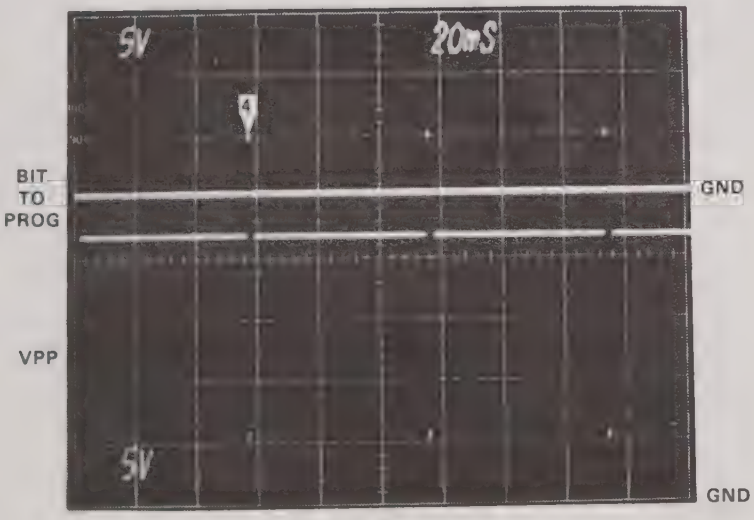
DATA I/O


5V
20mS
2
$\overline{E2}$
GND
TPW
VPP
5V
GND

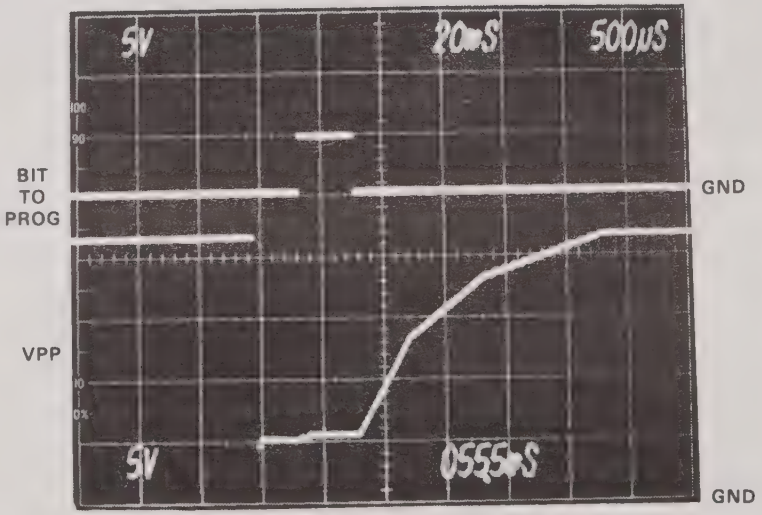
1


5V
20mS
500uS
$\overline{E2}$
GND
VPP
TPRC
VPP
VPPV
5V
0555mS
GND

2


5V
20mS
4
BIT
TO
PROG
GND
VPP
5V
GND

3


5V
20mS
500uS
BIT
TO
PROG
GND
VPP
5V
0555mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.0	5.0	6.0	V	
	VEE	9.0		15.0	V	
	TPW	50		70	ms	
	T_{PRC}	450	600	750	µs	See note 3
	T_F			100	µs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 85.*
2. *Load RAM with hex 01 for Family 86, and bit-to-prog waveform becomes bit-no-prog.*
3. *TPRC is measured from 6V to 15.5V.*
4. *Photos 8 and 9 are erase waveforms.*

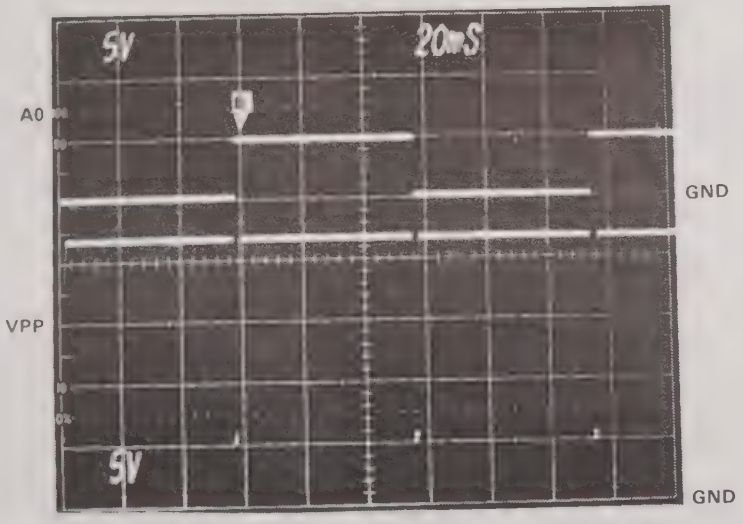
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

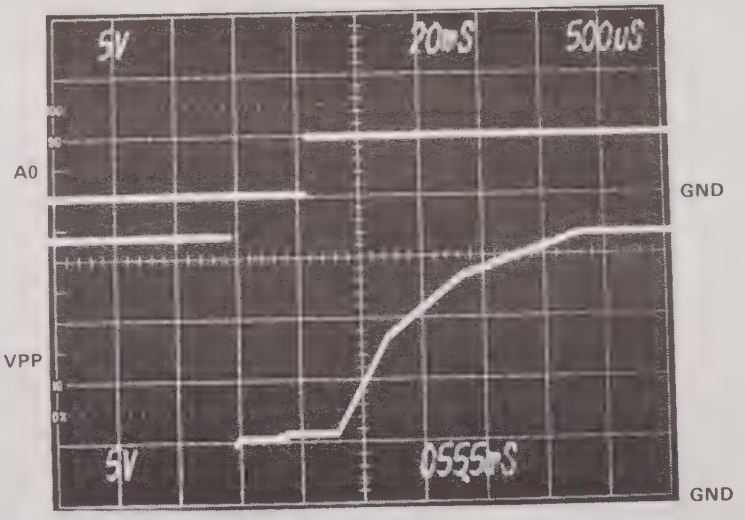
TIMING DIAGRAM

FAMILY CODES 85, 86

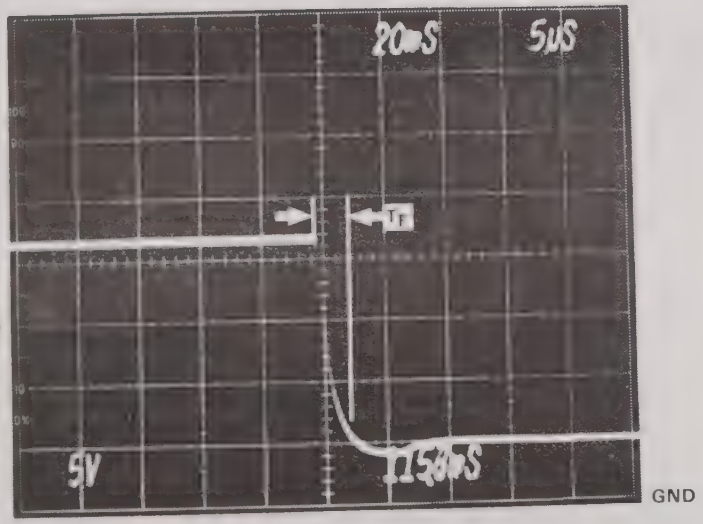
DATA I/O


5V
20mS
A0
GND
VPP
5V
GND

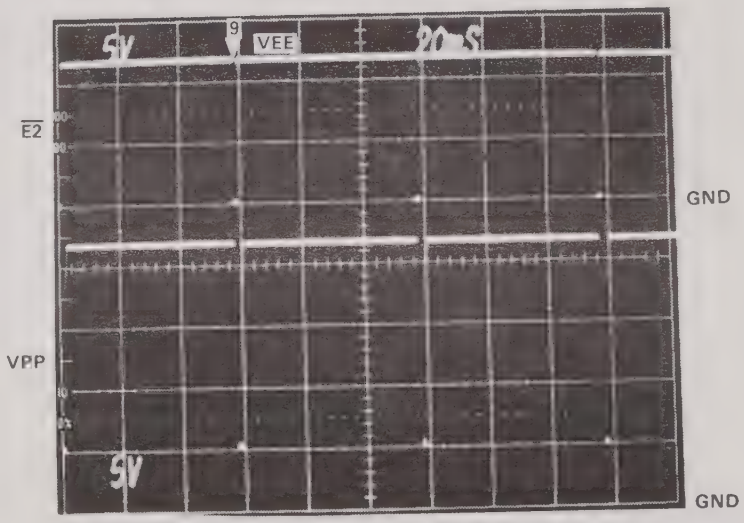
5


5V
20mS
500uS
A0
GND
VPP
5V
GND

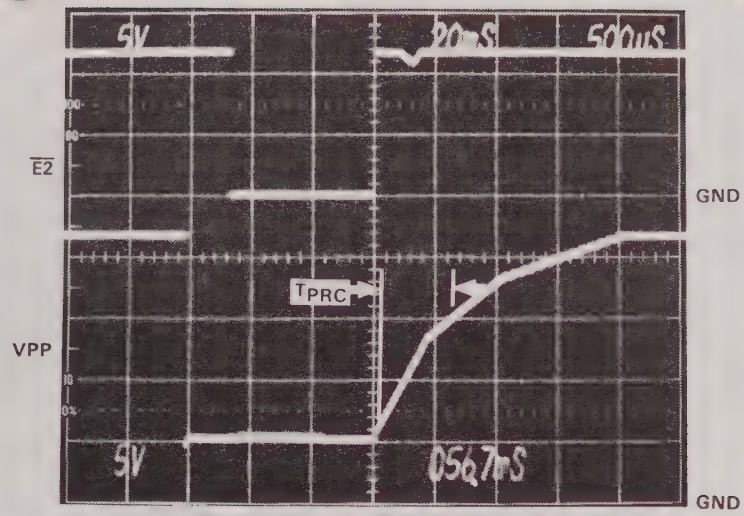
6


20mS
5uS
Tf
VPP
5V
GND

7


5V
9
VEE
20mS
E2
GND
VPP
5V
GND

8



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REVISIONS

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	ECN #5022	CTJ	3/84

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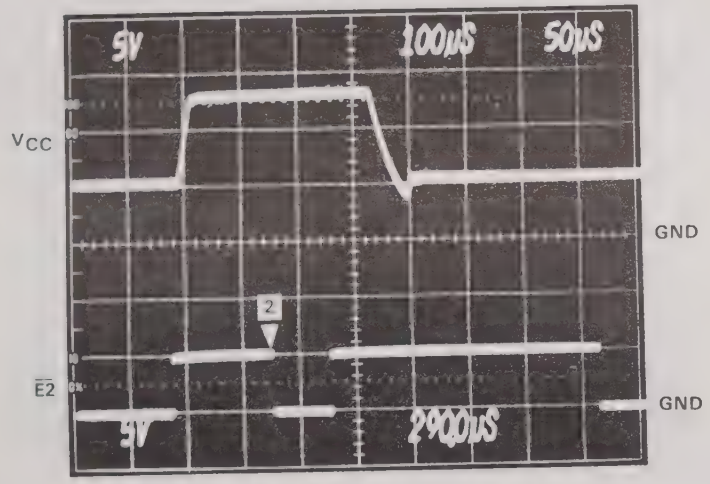
TIMING DIAGRAM

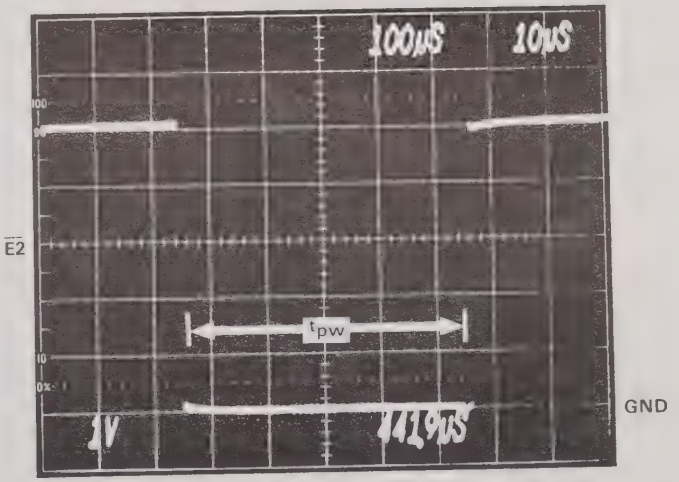
FAMILY CODES 85, 86

DATA I/O

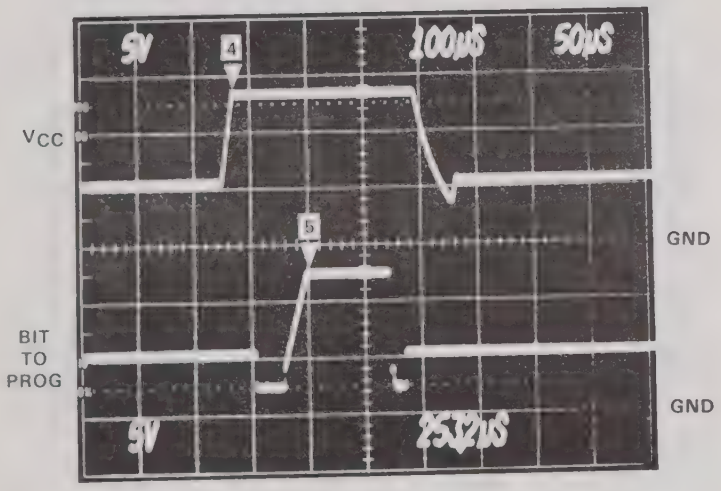
0526-1282


5V
100µS
50µS
VCC
GND
2
E2
GND
3V
2900µS

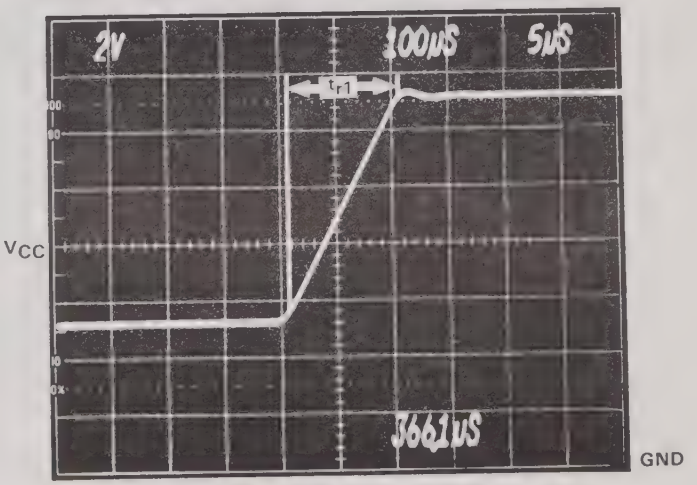
1


100µS
10µS
E2
tpw
GND
1V
1119µS

2


5V
4
100µS
50µS
VCC
GND
5
BIT
TO
PROG
GND
5V
2520µS

3


2V
100µS
5µS
tr1
VCC
GND
3661µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	12.5	12.5	13.0	V	
	V_{OP}	11.5	12.0	12.5	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{CCN}	4.75	5.0	5.25	V	
	t_{pw}	40	50	60	μs	
	t_{r1}	5		20	μs	
	t_{r2}	10		20	μs	
	Reject		1		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	0.4	0.5	0.6	V	701-1998/TP4
	HIGH LOAD	16.9	17.9	18.9	V	701-1998/TP2
	LOW LOAD	16.9	17.9	18.9	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	2.3	2.4	2.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	22.1	23.1	24.1	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 91.*
2. *Load RAM with hex 01 for Family 92.*

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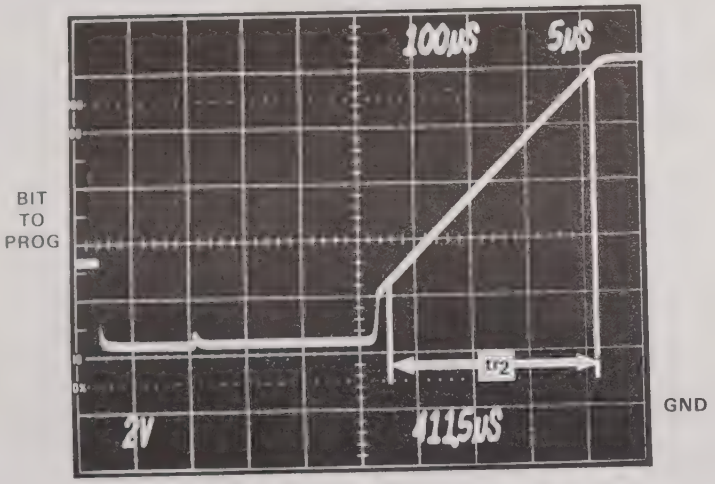
Sheet 1 of 2

TIMING DIAGRAM

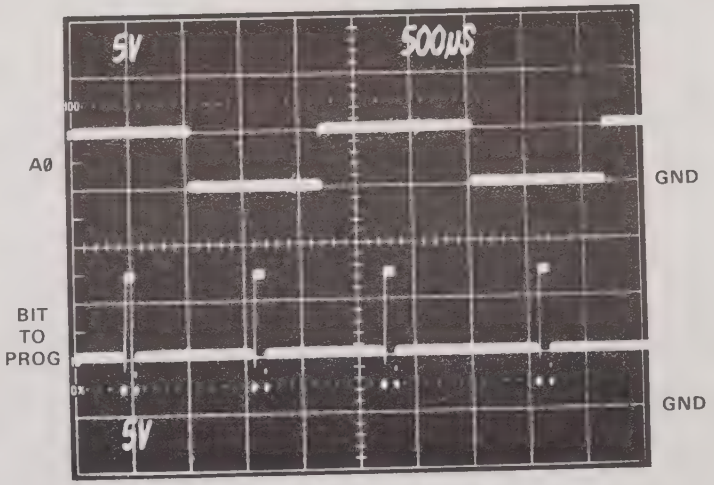
FAMILY CODES 91, 92

DATA I/O

0526/1282


100µS
5µS
BIT
TO
PROG
GND
tr2
2V
115µS

5


5V
500µS
A0
GND
BIT
TO
PROG
GND
5V

6

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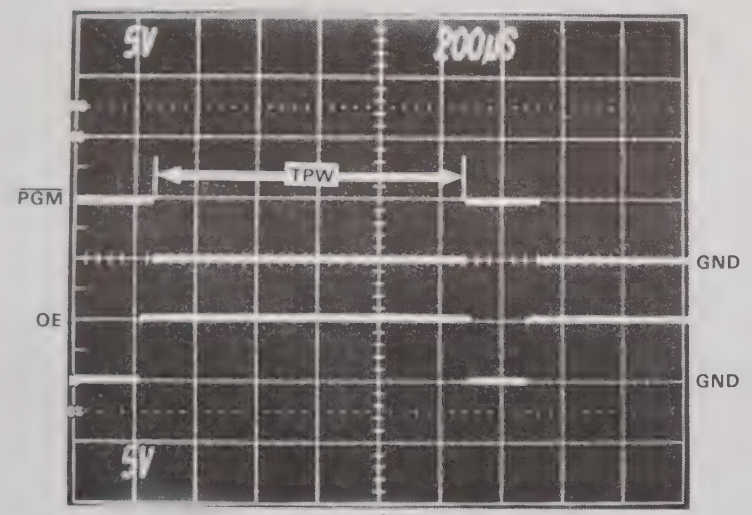
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

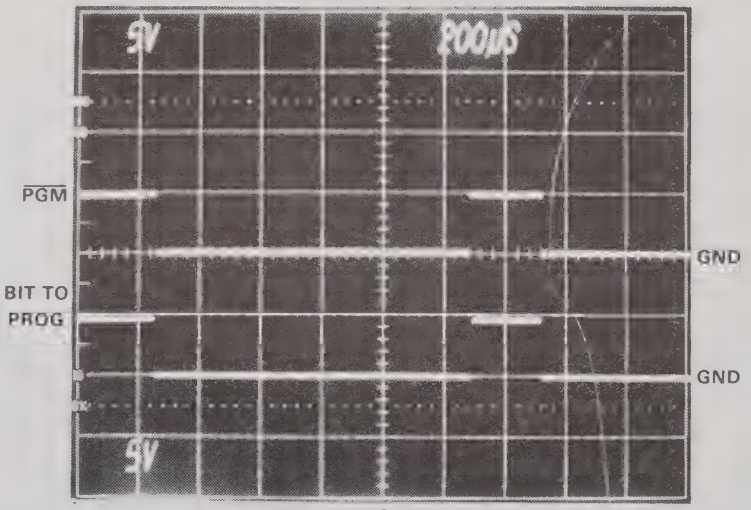
TIMING DIAGRAM

FAMILY CODES 91, 92

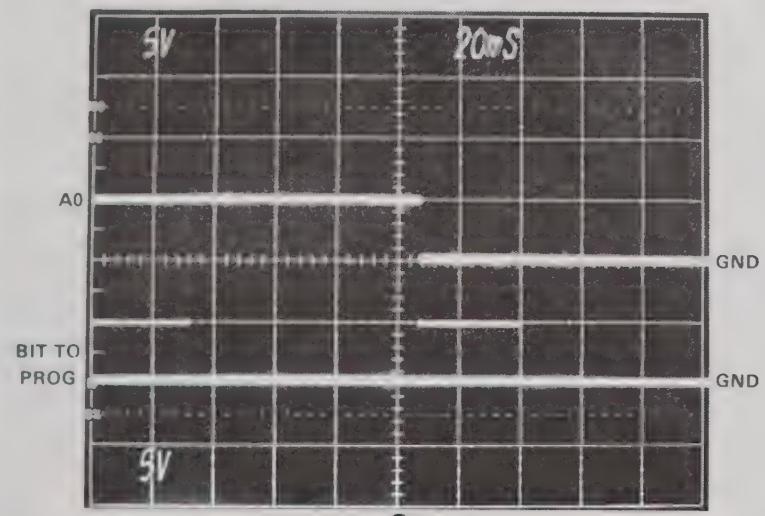
DATA I/O


5V
200µS
TPW
PGM
GND
OE
GND
5V

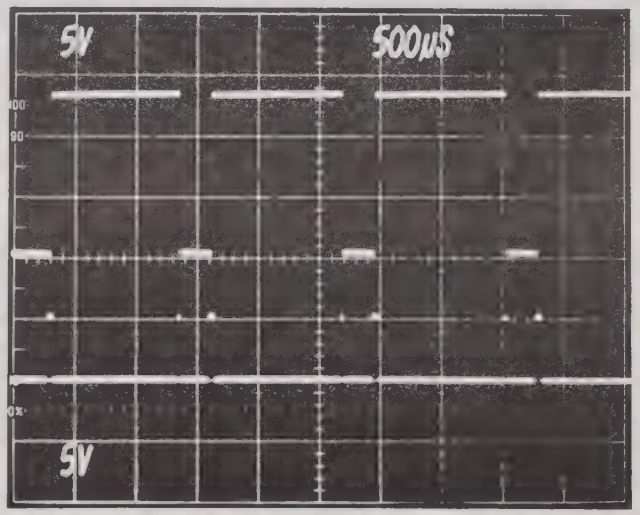
1


5V
200µS
PGM
GND
BIT TO
PROG
GND
5V

2


5V
20mS
A0
GND
BIT TO
PROG
GND
5V

3


5V
500µS
100
90
VPP
GND
PE
GND
0%
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.00	6.25	V	Not shown
	VOP					NA
	VPP	12.2	12.5	12.8	V	Not shown
	VPPV					NA
	TPW	0.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		25		Pulses	
	Overprogram		1		Pulse	See note 3
2ND PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
1ST PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 93.*
2. *Load RAM with hex 01 for Family 94, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 3 ms times the number of programming pulses required to program the location.*
4. *Photo 4 is for Pinout 24.*

REVISIONS

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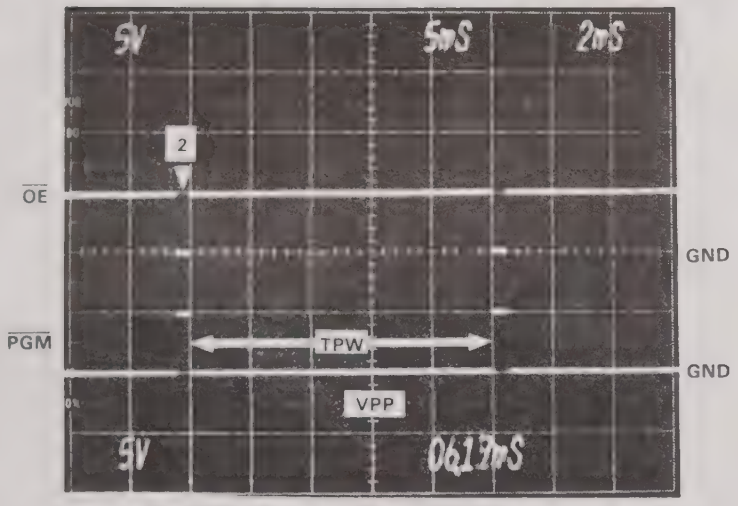
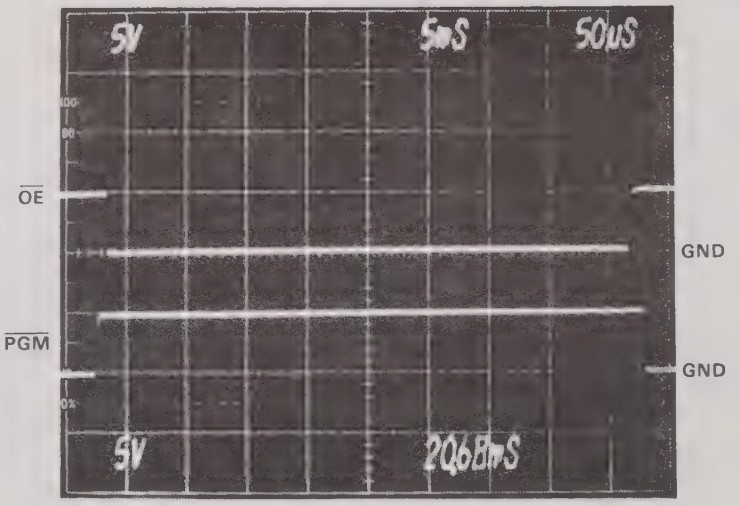
TIMING DIAGRAM

FAMILY CODES 93, 94

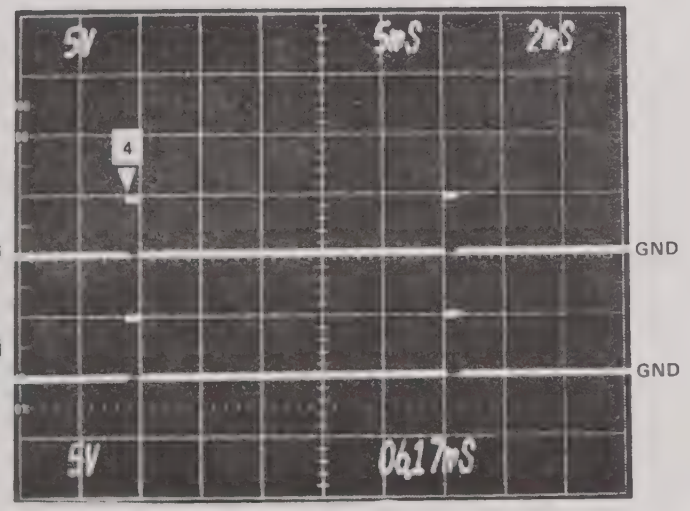
DATA I/O


5V
5mS
2mS
2
OE
GND
PGM
TPW
GND
VPP
5V
0617mS

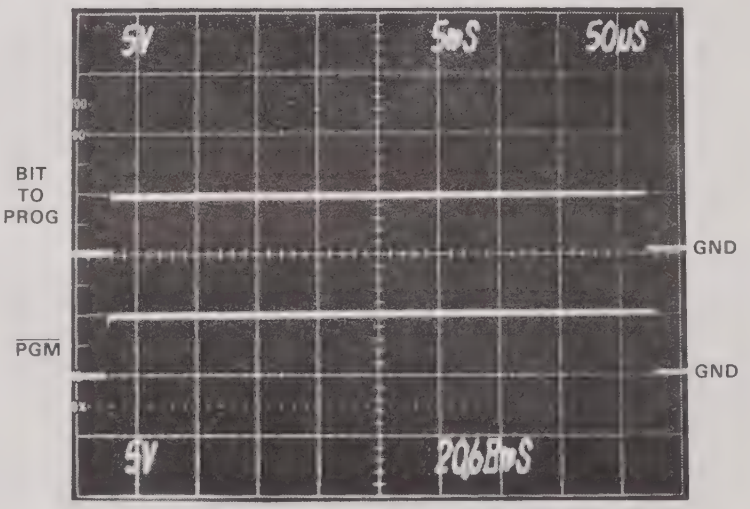
1


5V
5mS
50uS
OE
GND
PGM
GND
5V
2068mS

2


5V
5mS
2mS
4
BIT
TO
PROG
GND
PGM
GND
5V
0617mS

3


5V
5mS
50uS
BIT
TO
PROG
GND
PGM
GND
5V
2068mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.5	5.0	5.5	V	
	VPP	0.0	0.0	0.8	V	
	VEE	12.0	14.5	21.0	V	
	TPW	5.0	10.0	15.0	ms	
	TR				NA	
	TF				NA	
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS	V_{CC}	4.7	4.8	4.9	V	
VERIFY	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.4	22.4	23.4	V	701-1998/TP3
2ND PASS	V_{CC}	5.1	5.2	5.3	V	
VERIFY	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	6.9	7.9	8.9	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family A5.*
2. *Load RAM with hex 01 for Family A6, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photos 6 and 7 are erase waveforms.*

REVISIONS

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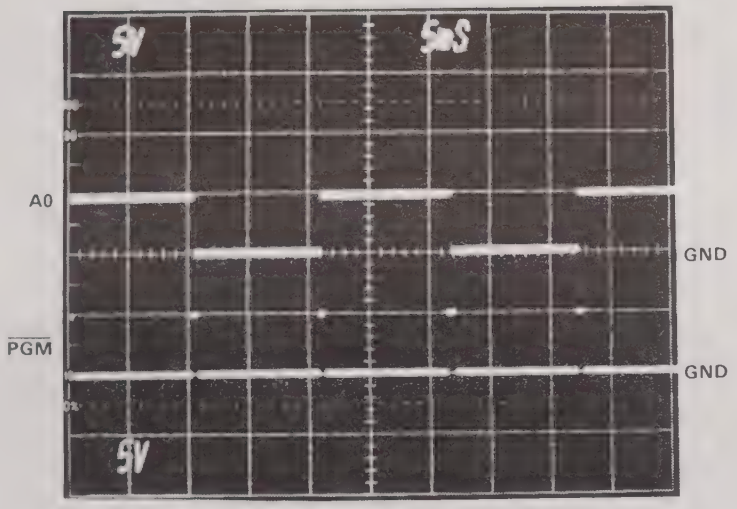
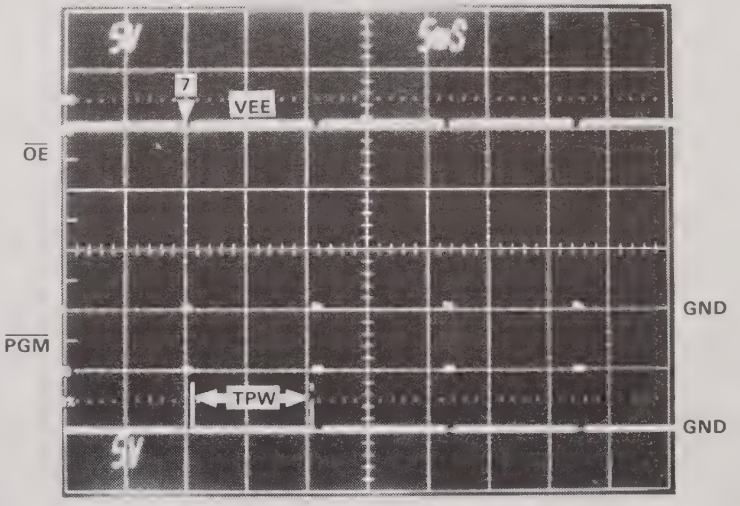
TIMING DIAGRAM

FAMILY CODES A5, A6

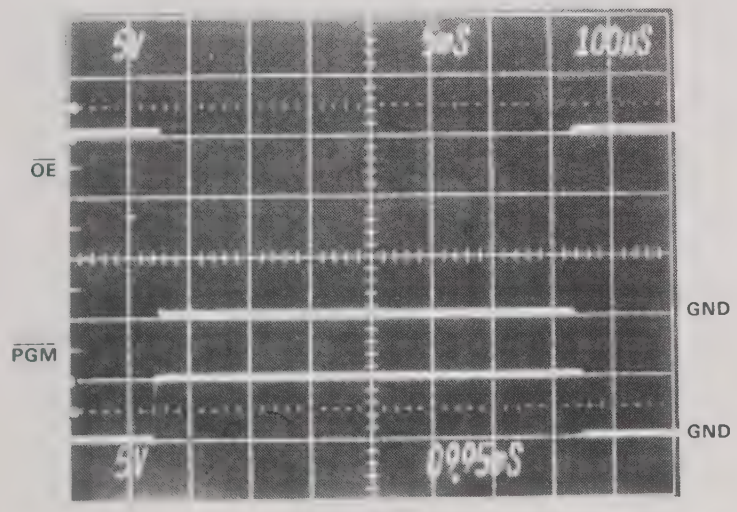
DATA I/O


5V
5mS
A0
GND
PGM
GND
5V

5


5V
5mS
7
VEE
OE
GND
PGM
TPW
GND
5V

6


5V
1mS
100uS
OE
GND
PGM
GND
5V
0.005S

7

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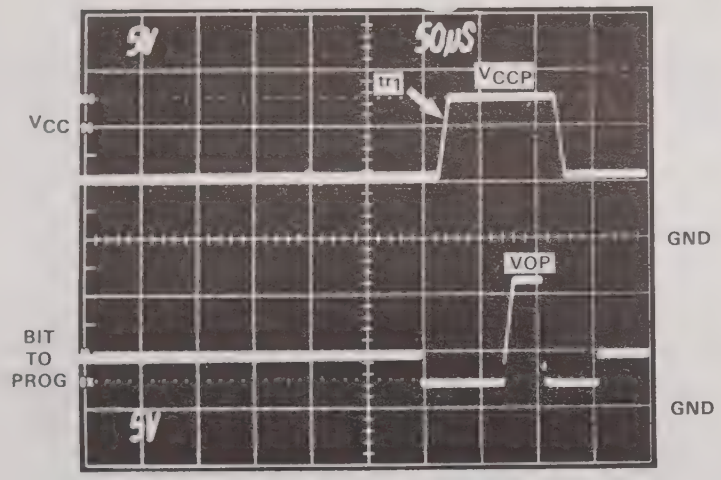
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

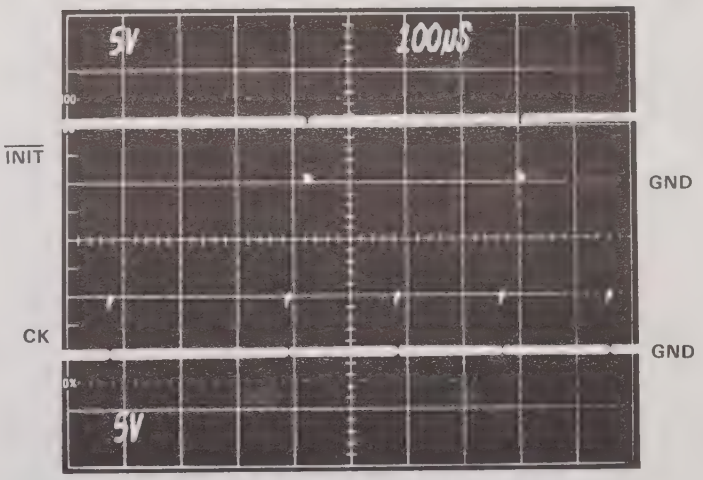
TIMING DIAGRAM

FAMILY CODES A5, A6

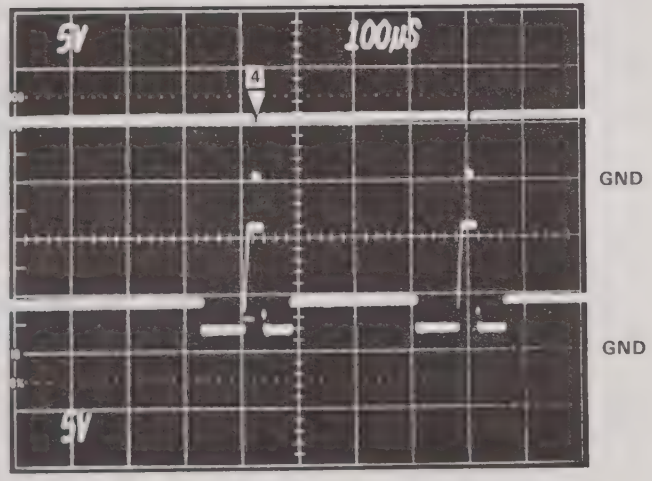
DATA I/O


5V
50µS
tr1
VCCP
VCC
GND
VOP
BIT
TO
PROG
GND
5V

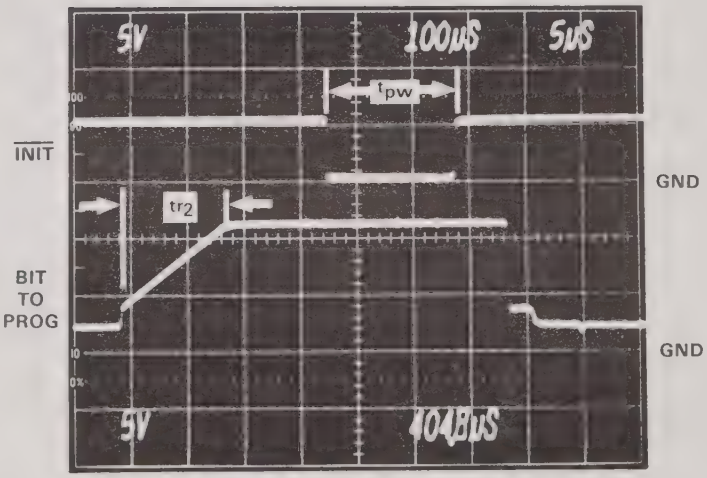
1


5V
100µS
INIT
GND
CK
GND
5V

2


5V
100µS
4
INIT
GND
BIT
TO
PROG
GND
5V

3


5V
100µS
5µS
tpw
INIT
GND
tr2
BIT
TO
PROG
GND
5V
40µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	11.6	11.8	12.0	V	
	V_{OP}	10.5	11.0	11.5	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	9.0	10.0	11.5	μs	
	t_{r1}	1		20.0	μs	See note 3.
	t_{r2}	1		15.0	μs	
	Reject		10		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.1	4.2	4.3	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	6.4	7.4	8.4	V	701-1998/TP2
	LOW LOAD	6.4	7.4	8.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	3.4	3.5	3.6	V	701-1998/TP4
	HIGH LOAD	7.7	8.7	9.7	V	701-1998/TP2
	LOW LOAD	7.7	8.7	9.7	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family A9.*
2. *Load RAM with hex 01 for Family AA.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

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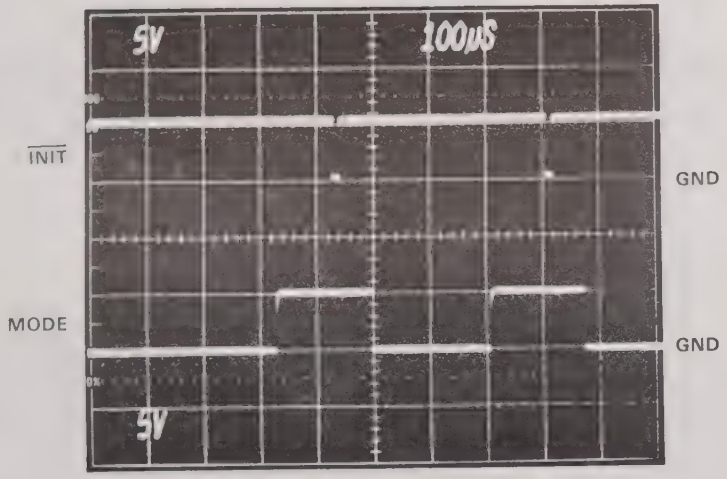
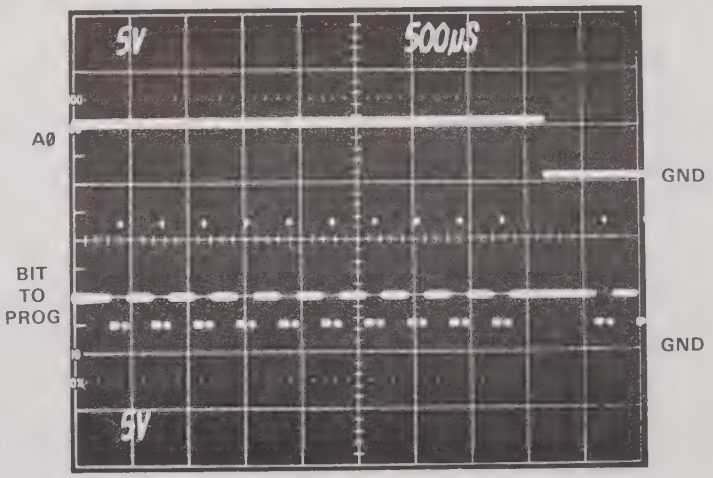
TIMING DIAGRAM

FAMILY CODES A9, AA

DATA I/O



5



6

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LTR	DESCRIPTION	P.E.	DATE
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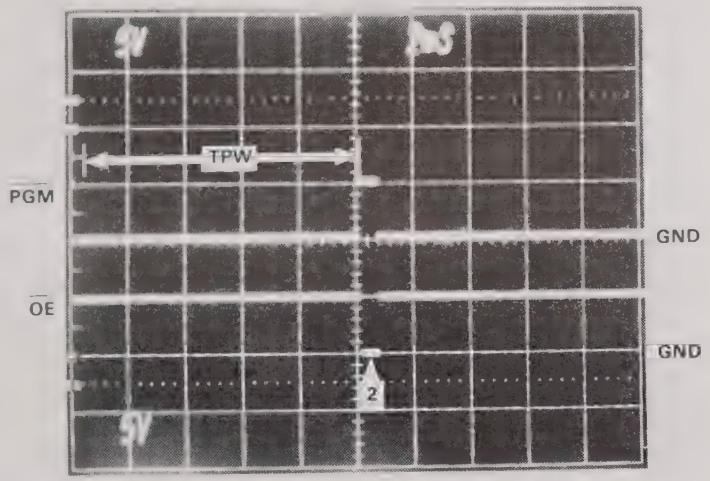
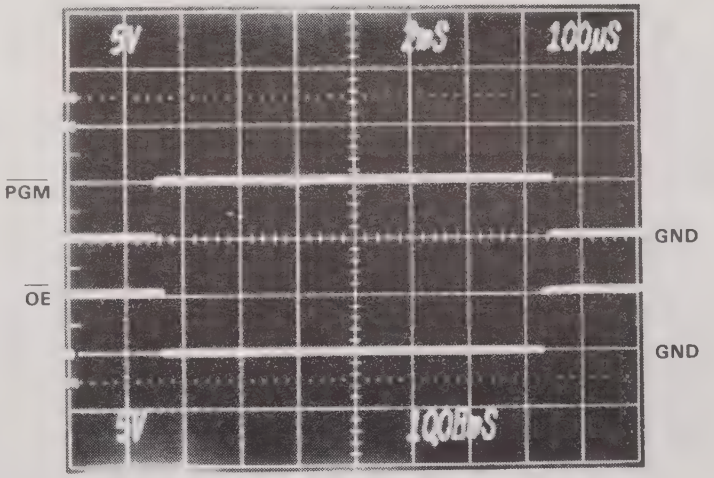
TIMING DIAGRAM

FAMILY CODES A9, AA

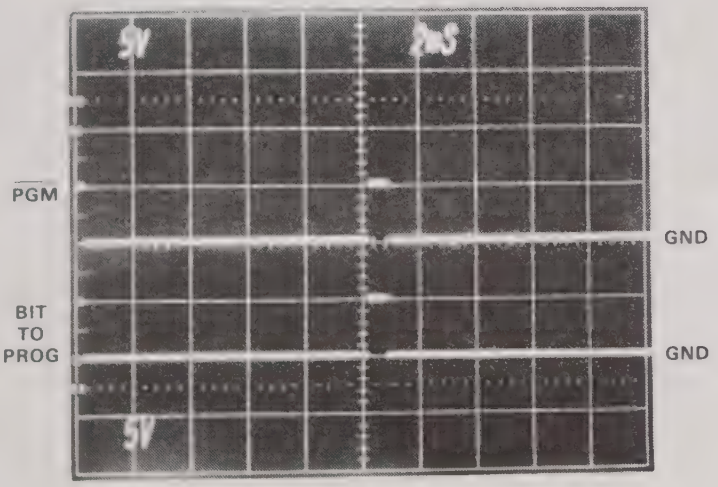
DATA I/O


5V
1mS
TPW
PGM
GND
OE
GND
2
5V

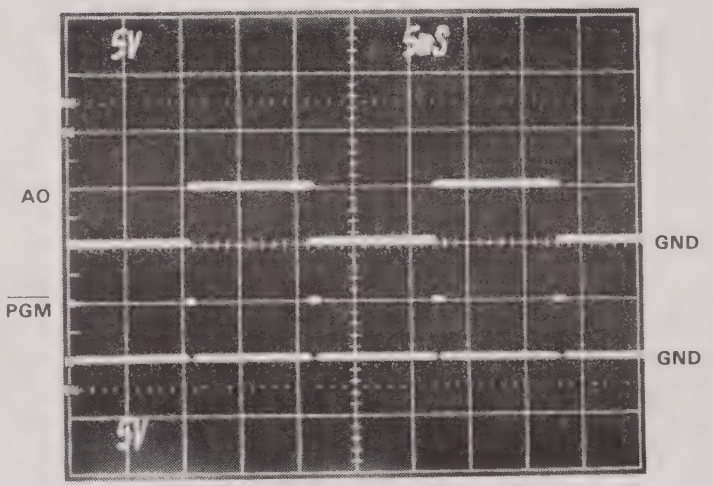
1


5V
1mS
100µS
PGM
GND
OE
GND
5V
100µS

2


5V
1mS
PGM
GND
BIT
TO
PROG
GND
5V

3


5V
5mS
AO
GND
PGM
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_{ew}	9.5	10.0	10.5	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.4	22.4	23.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	7.4	7.9	8.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family AB.*
2. *Photos 5 to 8 are chip erase waveforms.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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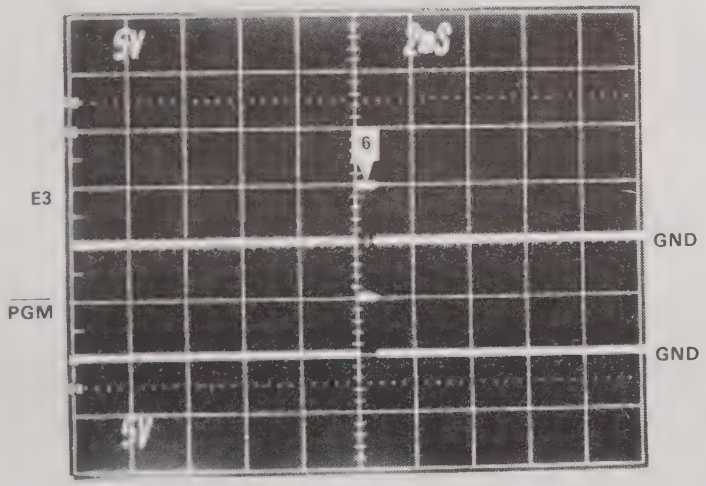
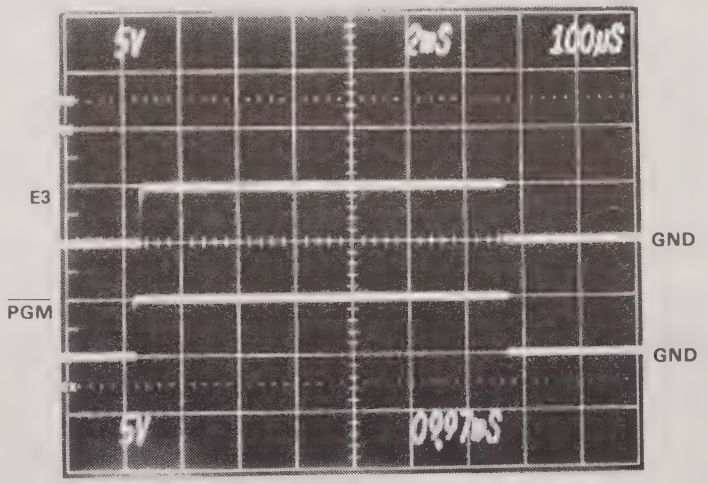
TIMING DIAGRAM

FAMILY CODES AB, AC

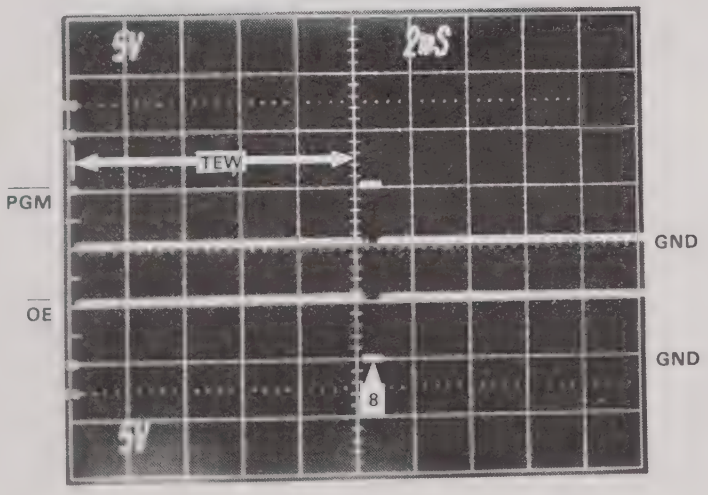
DATA I/O


5V
2mS
6
E3
GND
PGM
GND
5V

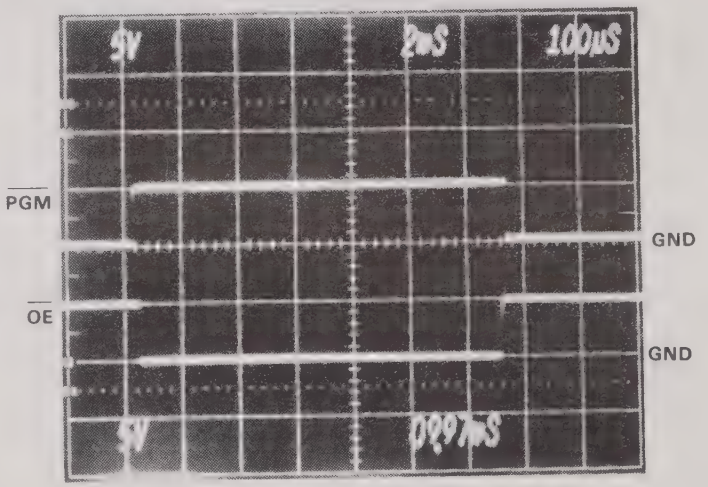
5


5V
2mS
100µS
E3
GND
PGM
GND
5V

6


5V
2mS
TEW
PGM
GND
OE
GND
8
5V

7


5V
2mS
100µS
PGM
GND
OE
GND
5V

8

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LTR	DESCRIPTION	P.E.	DATE
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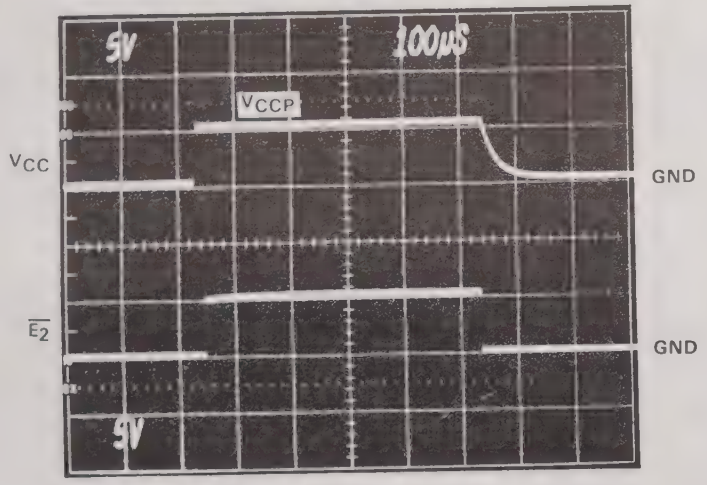
TIMING DIAGRAM

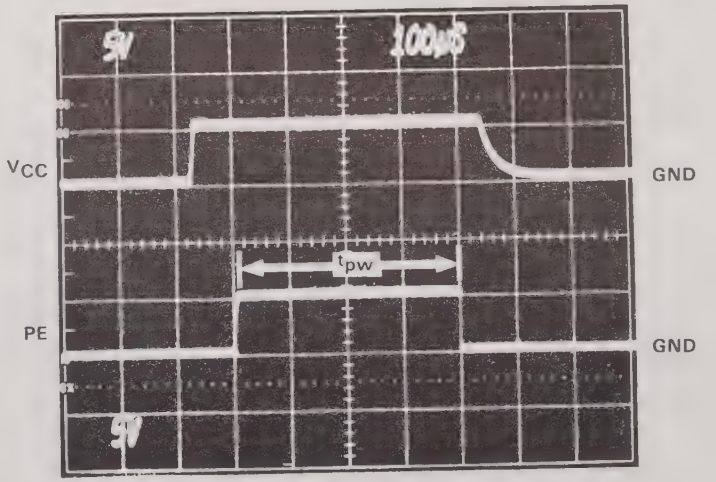
FAMILY CODES AB, AC

DATA I/O

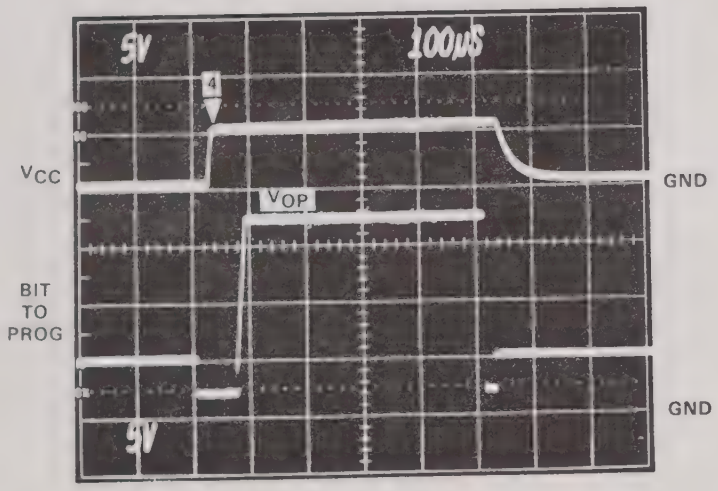
0526/1282


5V
100µS
VCCP
VCC
GND
$\overline{E_2}$
GND
5V

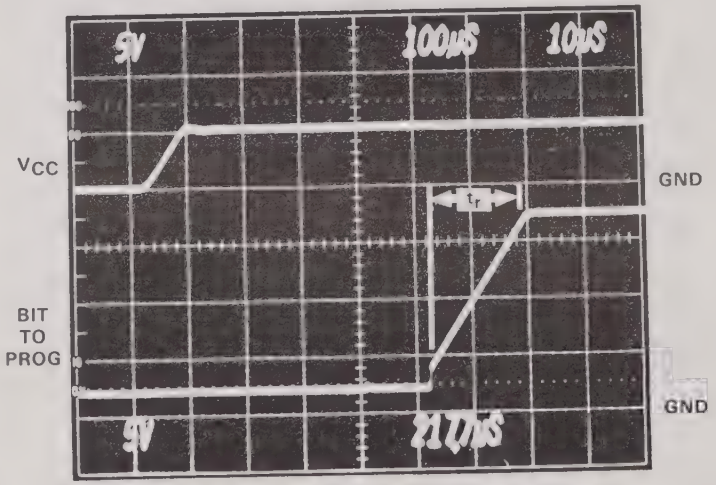
1


5V
100µS
VCC
GND
tpw
PE
GND
5V

2


5V
100µS
4
VCC
GND
VOP
BIT
TO
PROG
GND
5V

3


5V
100µS
10µS
VCC
GND
tr
BIT
TO
PROG
GND
5V
210µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	
	V_{OP}	16.0	17.0	18.0	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	300	400	500	μs	
	t_r	10		50	μs	
	Reject		1		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	1.4	1.5	1.6	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.7	5.2	5.7	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	1.4	1.5	1.6	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.7	5.2	5.7	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family AD.*
2. *Load RAM with hex 01 for Family AE.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

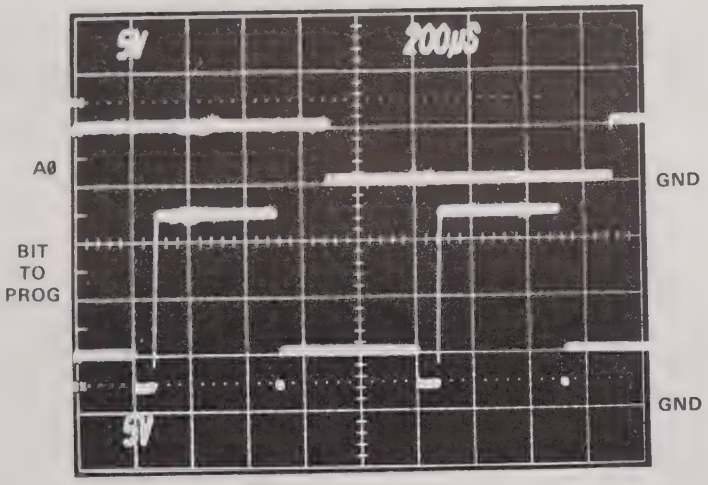
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

TIMING DIAGRAM

FAMILY CODES AD, AE

DATA I/O



5

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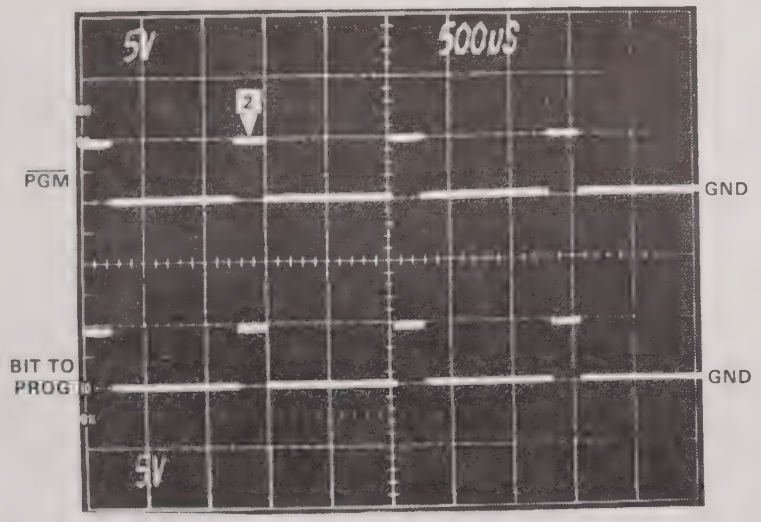
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022		

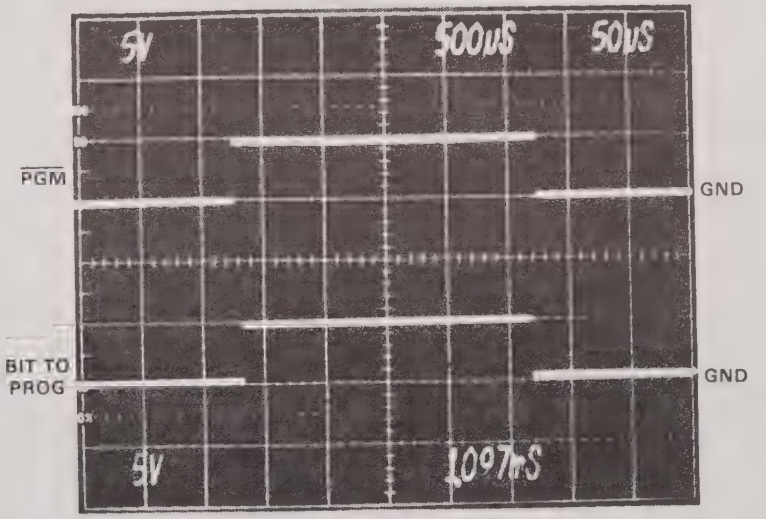
TIMING DIAGRAM

FAMILY CODES AD, AE

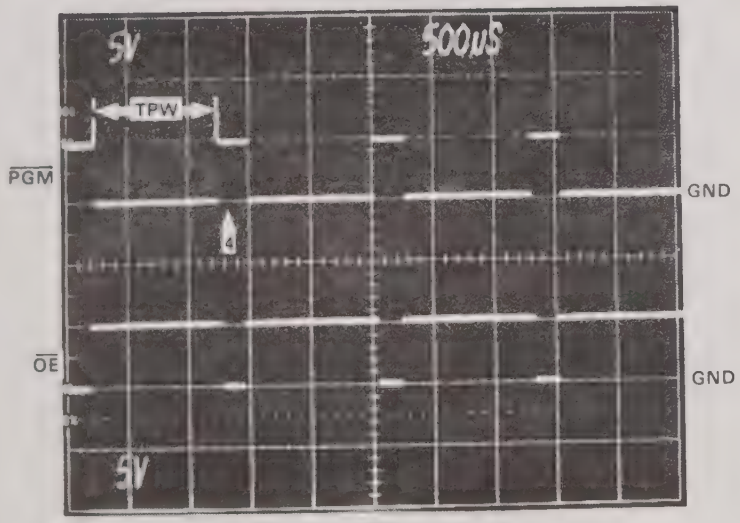
DATA I/O


5V
500uS
2
PGM
GND
BIT TO PROG
GND
5V

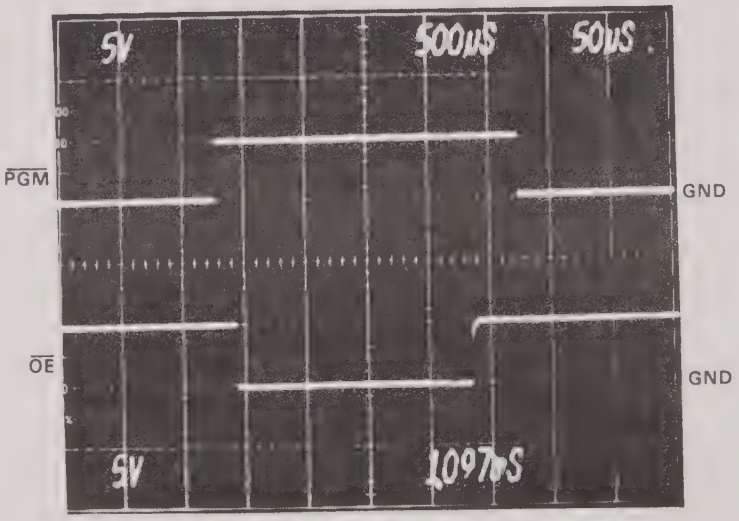
1


5V
500uS
50uS
PGM
GND
BIT TO PROG
GND
5V
1.097mS

2


5V
500uS
TPW
PGM
GND
4
OE
GND
5V

3


5V
500uS
50uS
PGM
GND
OE
GND
5V
1.097mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	21.0	21.5	22.0	V	Not shown
	V_{PPV}					N.A.
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSE	
	Overprogram		1		PULSE	See note 3
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family AF.*
2. *Load RAM with hex 01 for Family BO and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 2 ms long; see photos 6 and 7.*

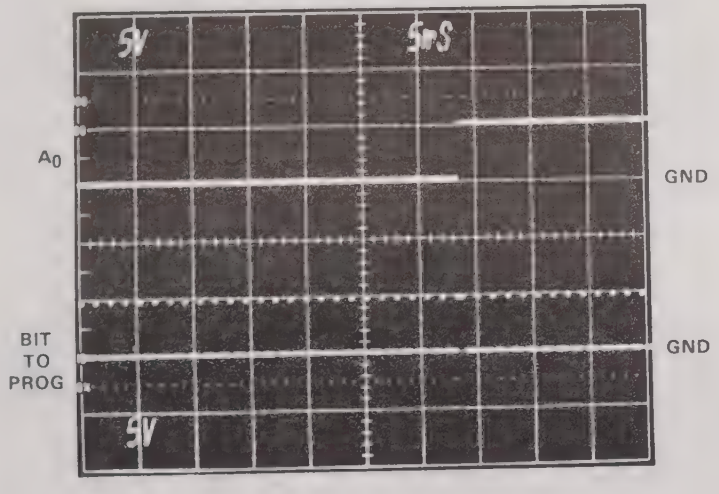
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

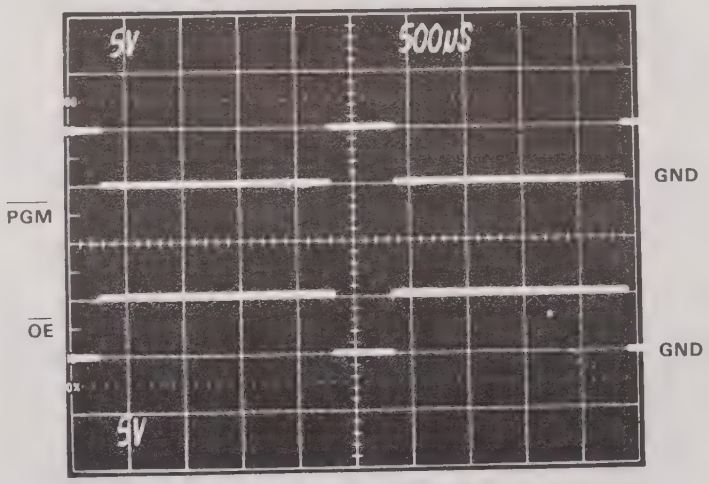
TIMING DIAGRAM

FAMILY CODES AF, BO

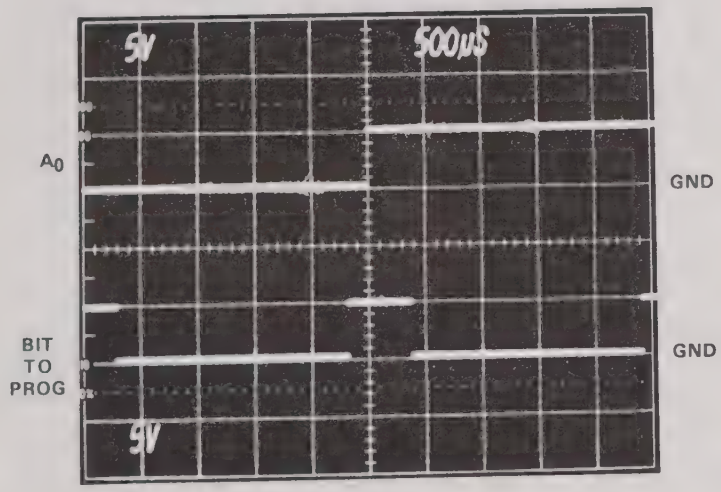
DATA I/O


5V
5mS
A0
GND
BIT
TO
PROG
GND
5V

5


5V
500µS
GND
PGM
OE
GND
5V

6


5V
500µS
A0
GND
BIT
TO
PROG
GND
5V

7

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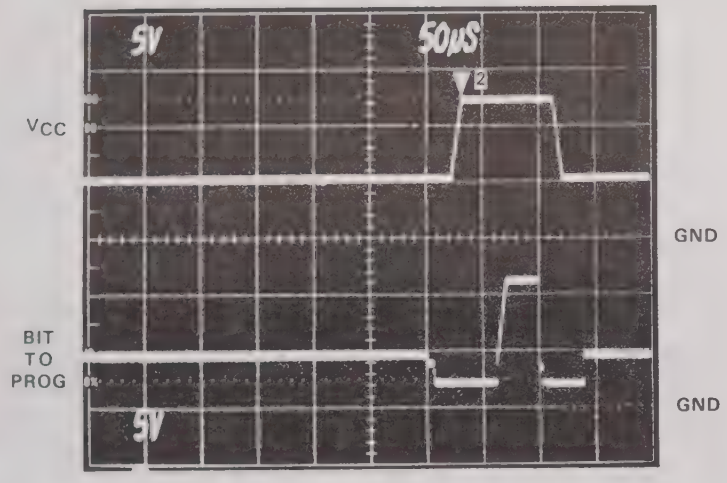
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

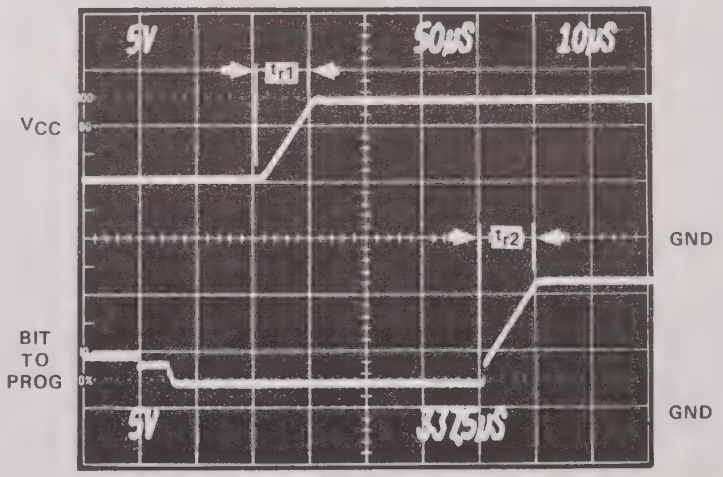
TIMING DIAGRAM

FAMILY CODES AF, BO

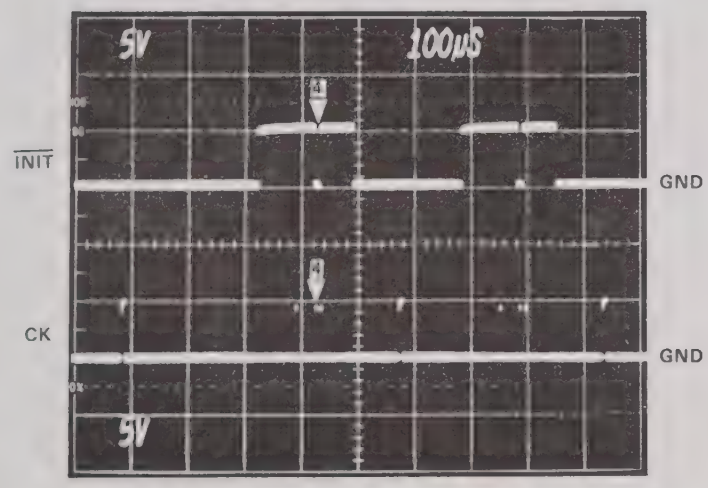
DATA I/O


5V
50µS
2
VCC
GND
BIT
TO
PROG
GND
5V

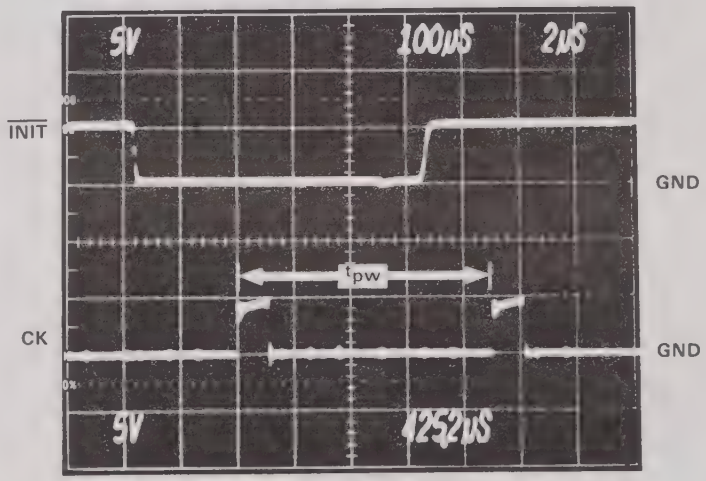
1


5V
50µS
10µS
tr1
VCC
tr2
GND
BIT
TO
PROG
GND
5V
3.75µS

2


5V
100µS
1
INIT
GND
2
CK
GND
5V

3


5V
100µS
2µS
INIT
GND
tpw
CK
GND
5V
125µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	11.6	11.8	12.0	V	
	V_{OP}	10.5	11.0	11.5	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	9.0	10.0	11.5	*us*	
	t_{r1}	1.0		20.0	*us*	See Note 3
	t_{r2}	1.0		15.0	*us*	
	t_f					N.A.
	Reject		10		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.1	4.2	4.3	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	6.4	7.4	8.4	V	701-1998/TP2
	LOW LOAD	6.4	7.4	8.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	3.4	3.5	3.6	V	701-1998/TP4
	HIGH LOAD	7.7	8.7	9.7	V	701-1998/TP2
	LOW LOAD	7.7	8.7	9.7	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family B1.*
2. *Load RAM with hex 01 for Family B2.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

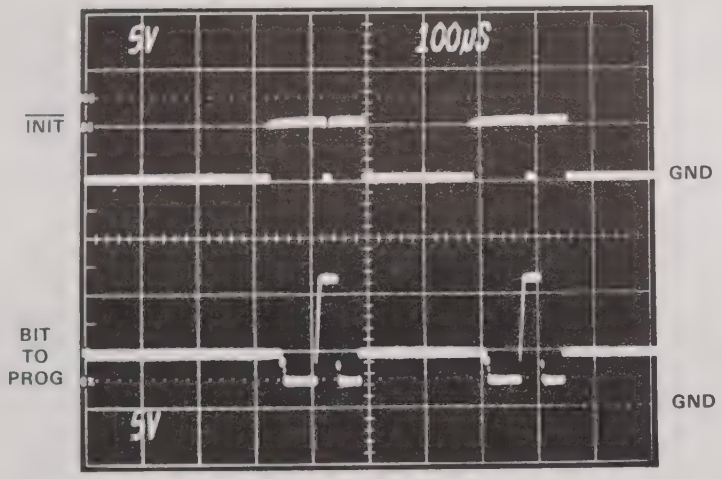
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

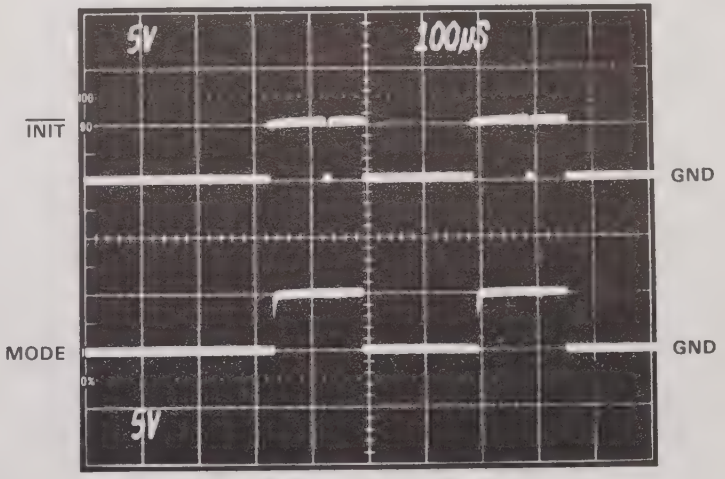
TIMING DIAGRAM

FAMILY CODES B1, B2

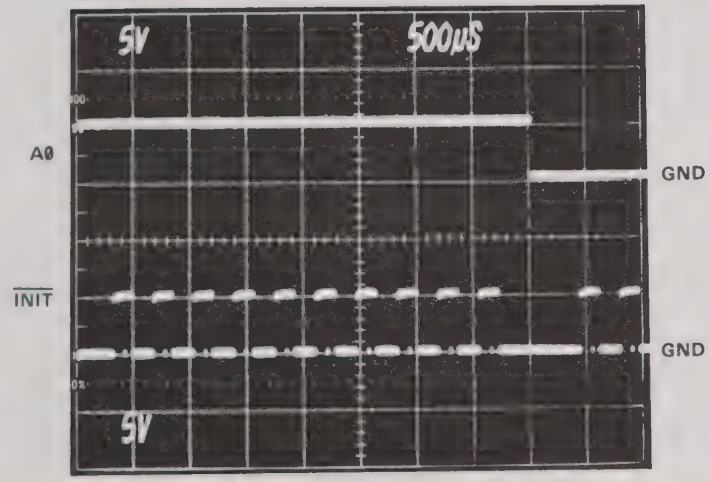
DATA I/O


5V
100µS
INIT
GND
BIT
TO
PROG
GND
5V

5


5V
100µS
INIT
GND
MODE
GND
5V

6


5V
500µS
A0
GND
INIT
GND
5V

7

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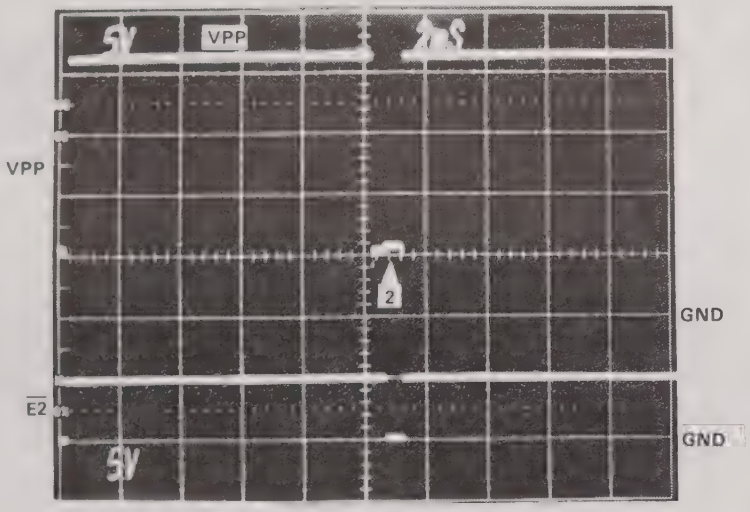
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

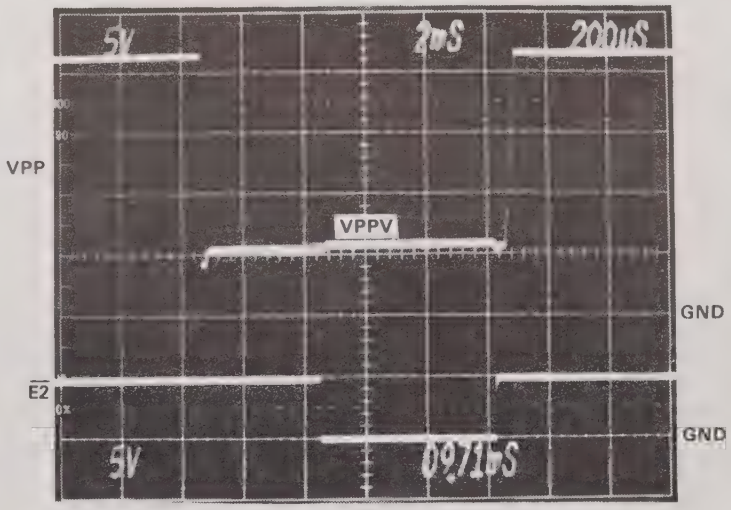
TIMING DIAGRAM

FAMILY CODES B1, B2

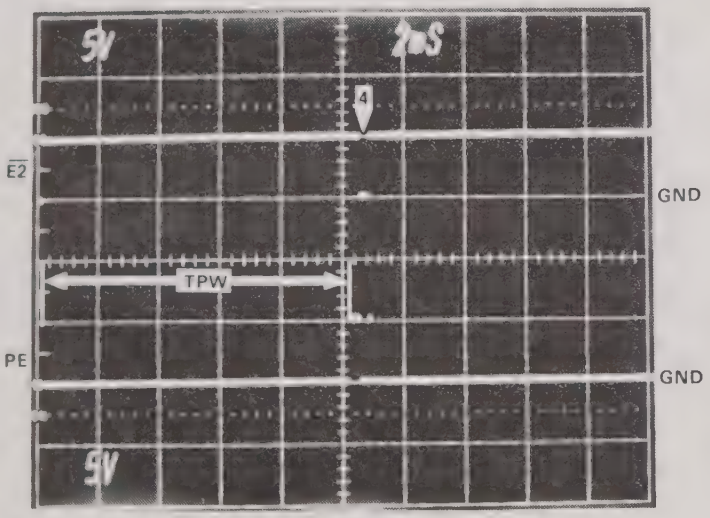
DATA I/O


5V
VPP
2mS
VPP
2
GND
E2
GND
5V

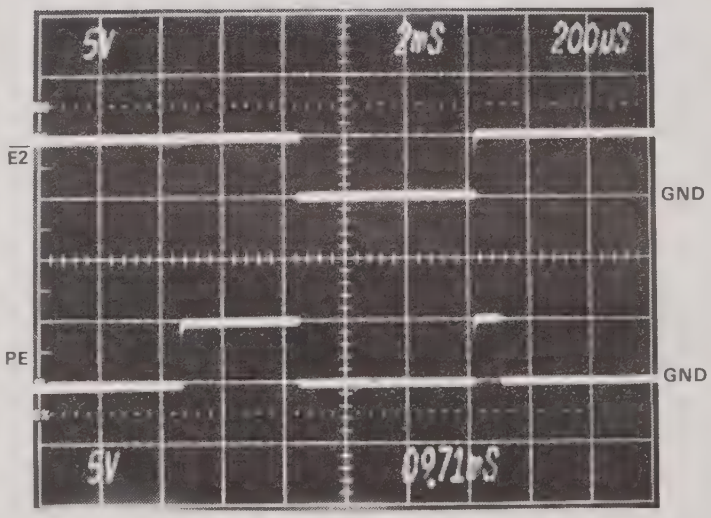
1


5V
2mS
200uS
VPP
VPPV
GND
E2
GND
5V
09.71mS

2


5V
2mS
4
E2
GND
TPW
PE
GND
5V

3


5V
2mS
200uS
E2
GND
PE
GND
5V
09.71mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	VEE	9.0	12.0	15.0	V	
	TPW	9.0		15.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family B3.*
2. *Load RAM with hex 01 for Family B4 and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Chip erase waveforms are photos 8 and 9.*
4. *Byte erase waveforms are photos 10 and 11.*

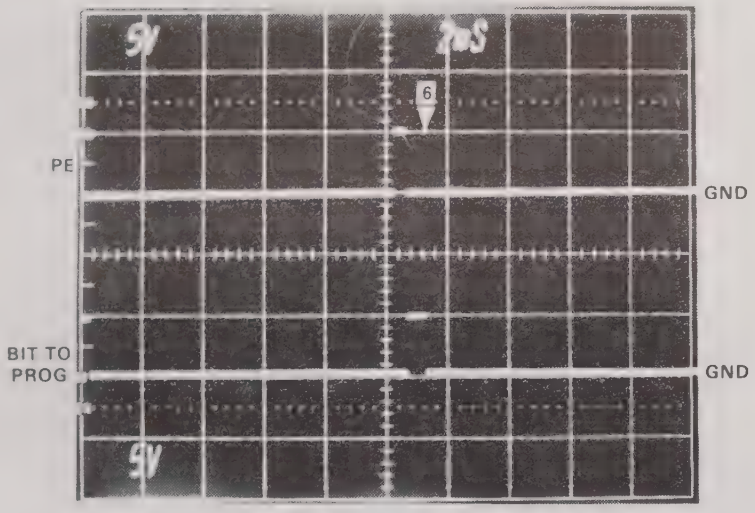
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

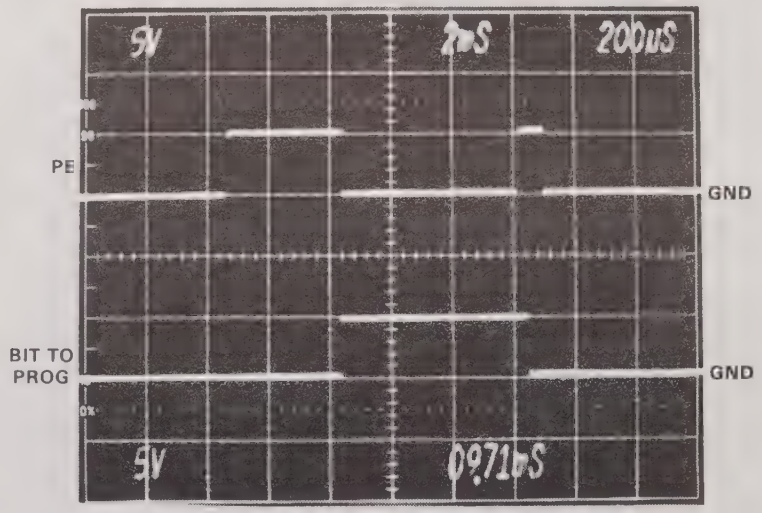
TIMING DIAGRAM

FAMILY CODES B3, B4

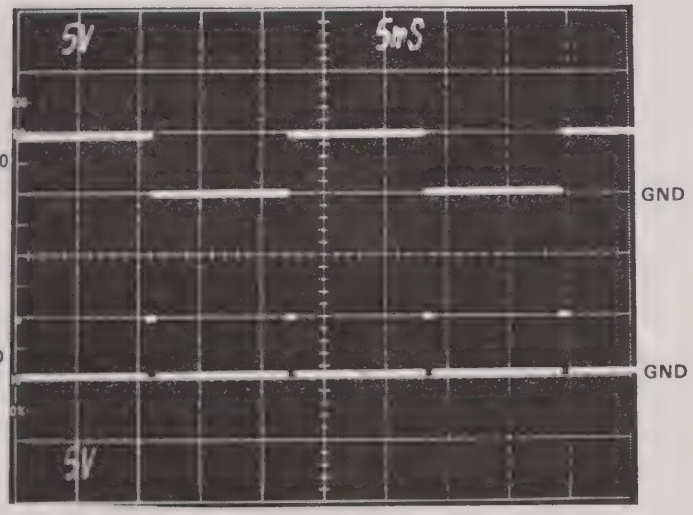
DATA I/O


5V
2mS
6
PE
GND
BIT TO
PROG
GND
5V

5


5V
2mS
200uS
PE
GND
BIT TO
PROG
GND
5V
0971uS

6


5V
5mS
A0
GND
BIT TO
PROG
GND
5V

7

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

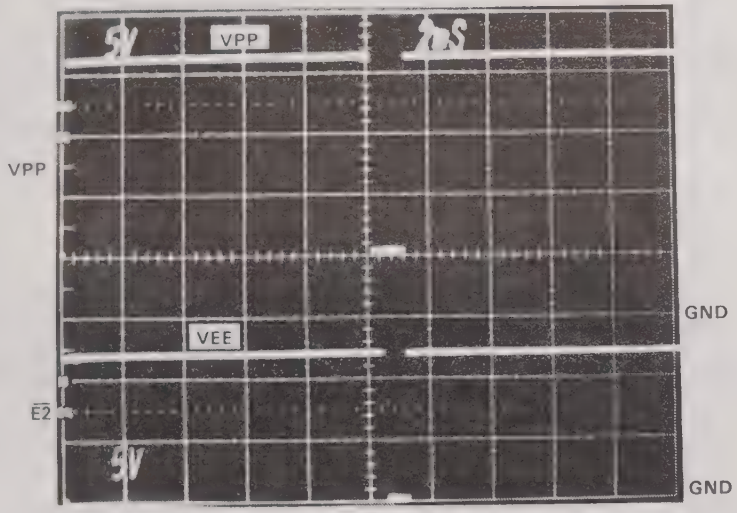
Sheet 2 of 3

TIMING DIAGRAM

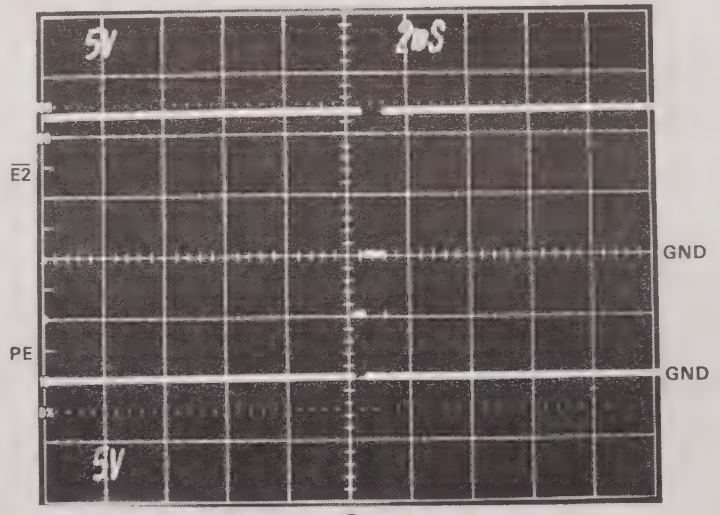
FAMILY CODES B3, B4

DATA I/O

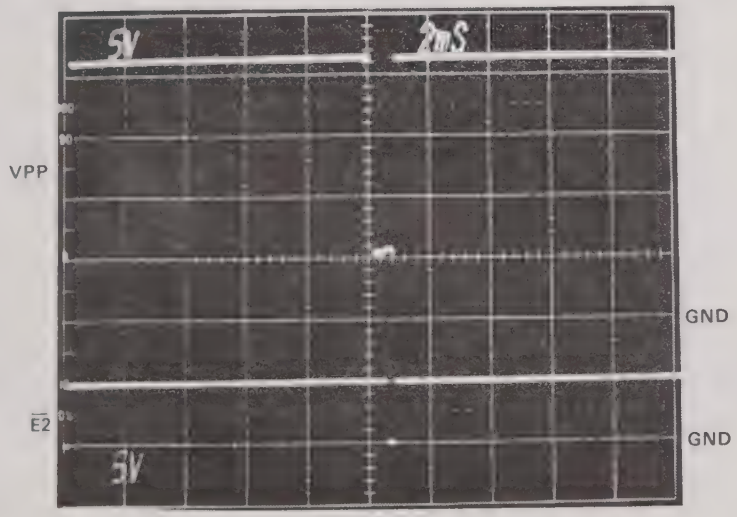
0526/1282


5V
VPP
2mS
VPP
VEE
GND
E2
5V
GND

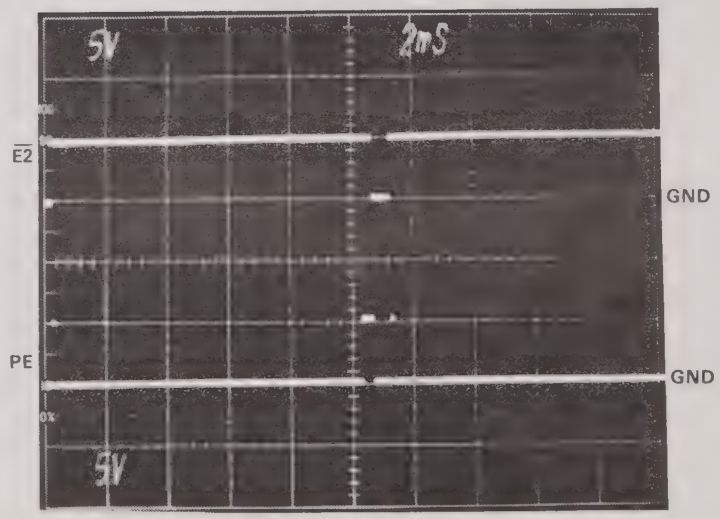
8


5V
2mS
E2
GND
PE
GND
5V

9


5V
2mS
VPP
GND
E2
GND
5V

10


5V
2mS
E2
GND
PE
GND
5V

11

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

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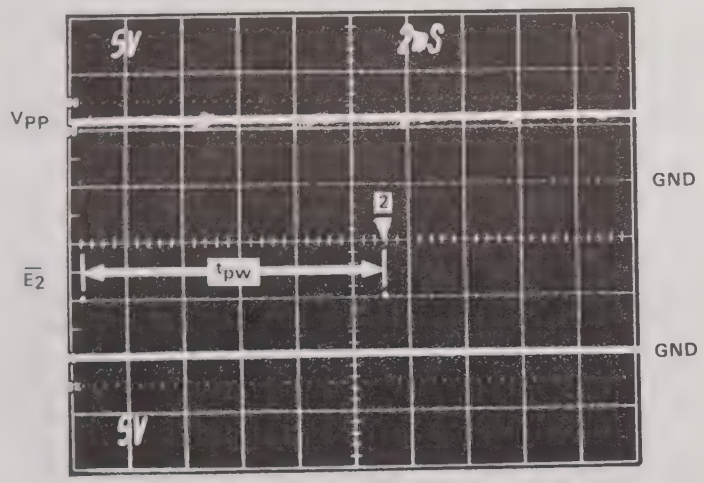
TIMING DIAGRAM

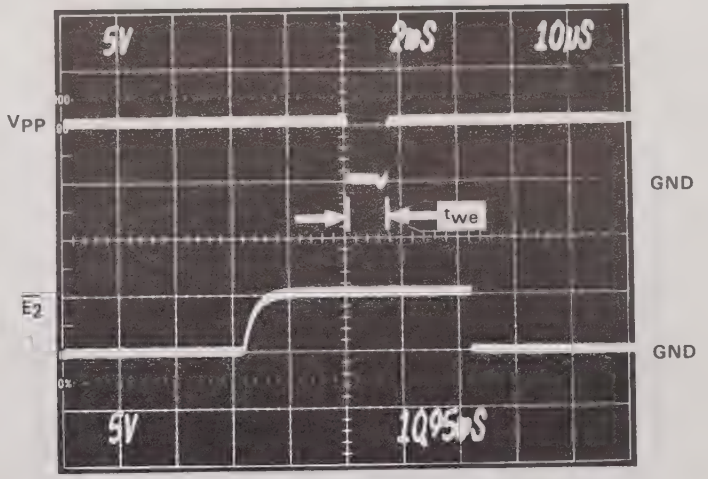
FAMILY CODES B3, B4

DATA I/O

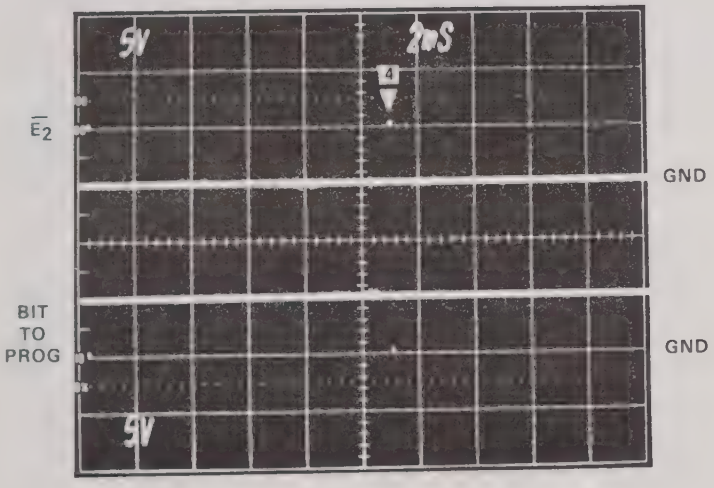
0526/1282


5V
2mS
VPP
GND
2
$\overline{E_2}$
tpw
GND
5V

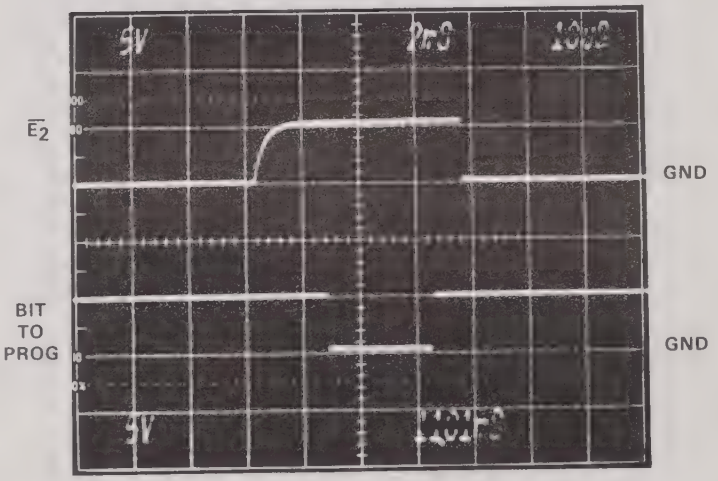
1


5V
2mS
10μS
VPP
GND
twe
$\overline{E_2}$
GND
5V

2


5V
2mS
4
$\overline{E_2}$
GND
BIT
TO
PROG
GND
5V

3


5V
$\overline{E_2}$
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EP}	20.5	21.0	21.5	V	
	V_{EE}	11.5	12.0	12.5	V	
	t_{we}	150			ns	
	t_{pw}	9	10		ms	
	t_r					N.A.
	t_{ew}	9	10	15	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.3	0.4	0.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.1	22.1	23.1	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	6.6	7.1	7.6	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family B7.*
2. *Load RAM with hex 01 for Family B8.*
3. *Photo 6 shows erase pulse.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/24

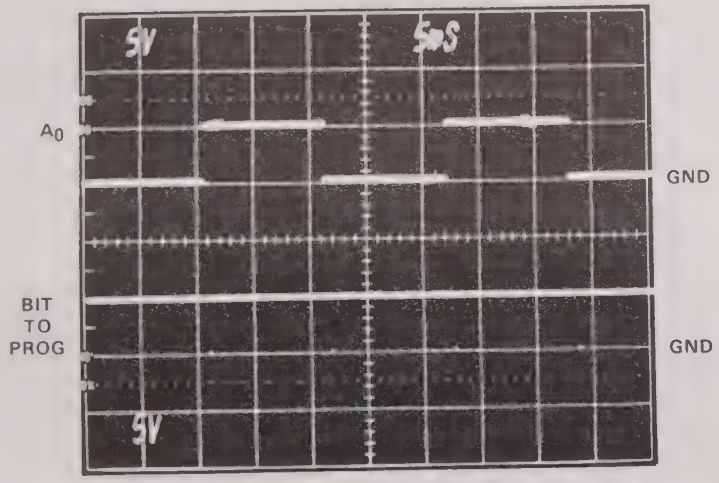
Sheet 1 of 2

TIMING DIAGRAM

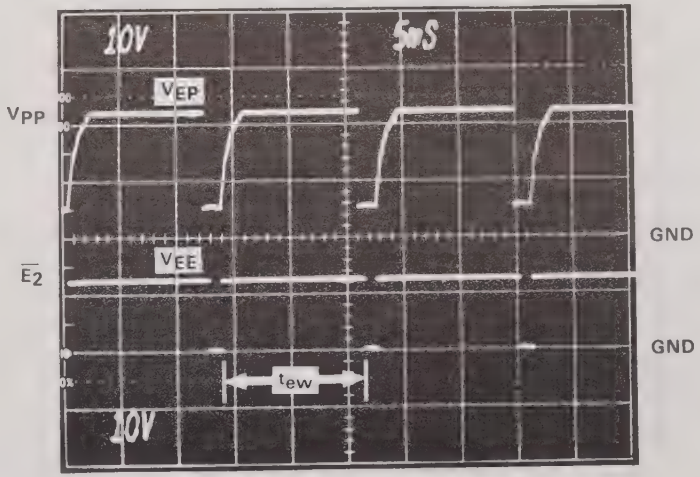
FAMILY CODES B7, B8

DATA I/O

0526/1282


5V
5mS
A_0
GND
BIT
TO
PROG
GND
5V

5


10V
5mS
V_{EP}
V_{PP}
GND
V_{EE}
$\overline{E_2}$
GND
t_{ew}
10V

6

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

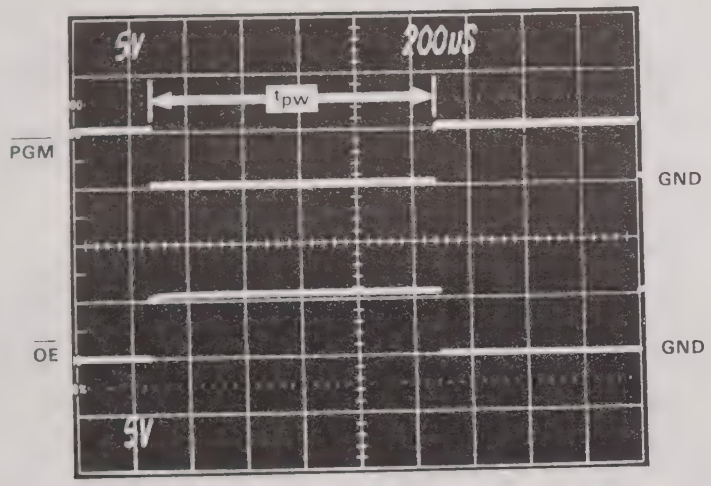
Sheet 2 of 2

TIMING DIAGRAM

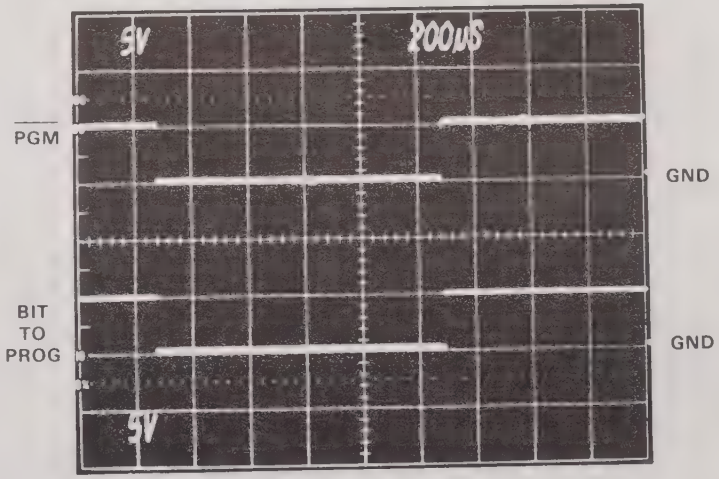
FAMILY CODES B7, B8

DATA I/O

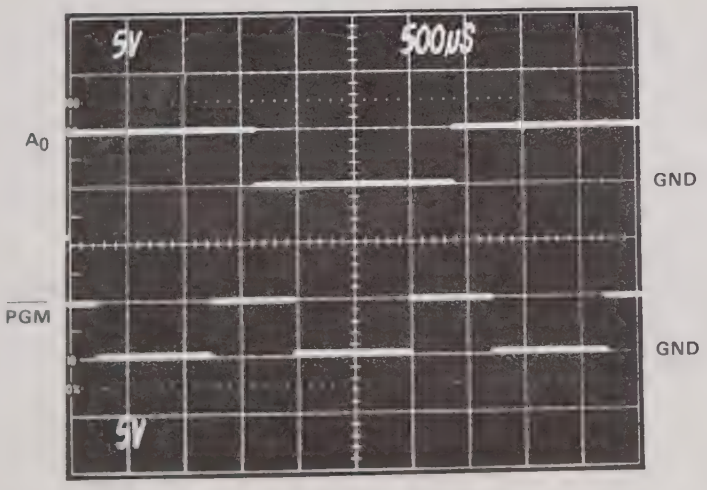
0526/1282


5V
200uS
t_{pw}
PGM
GND
OE
GND
5V

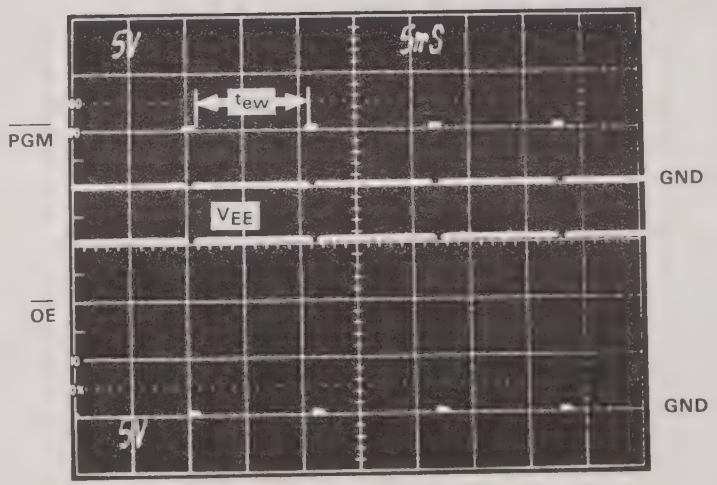
1


5V
200uS
PGM
GND
BIT
TO
PROG
GND
5V

2


5V
500uS
A_0
GND
PGM
GND
5V

3


5V
5mS
t_{ew}
PGM
GND
V_{EE}
OE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EE}	14.0	14.5	15.0	V	
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_{ew}	9.5	10.0	10.5	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.4	22.4	23.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	7.4	7.9	8.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family B9.*
2. *Photo 4 is chip erase.*

REVISIONS

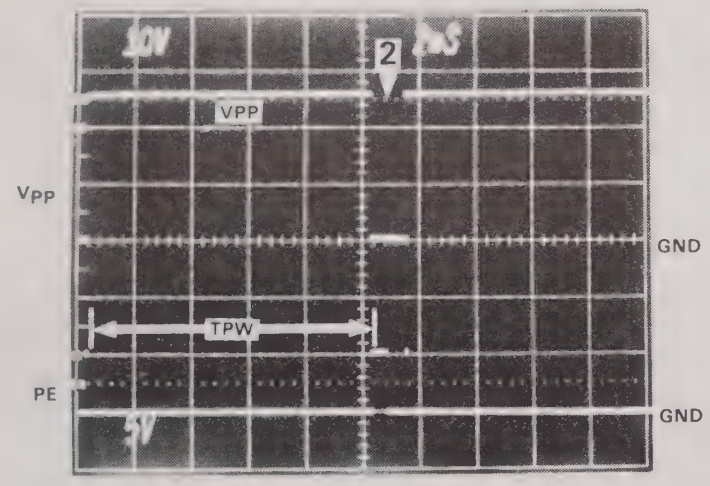
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

Sheet 1 of 1

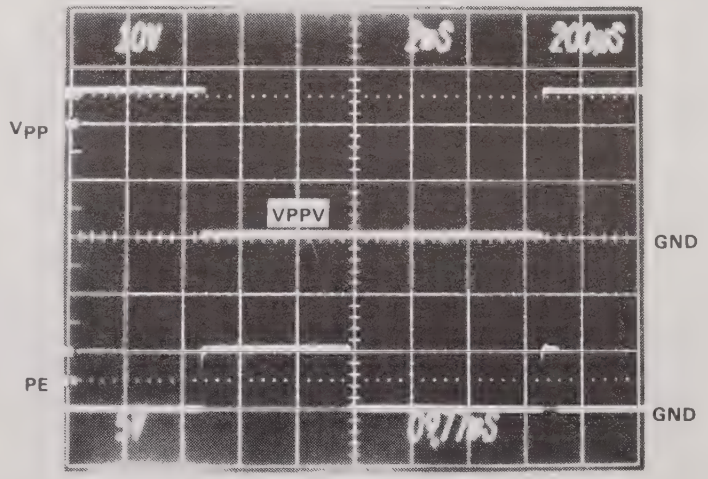
TIMING DIAGRAM

FAMILY CODES B9, BA

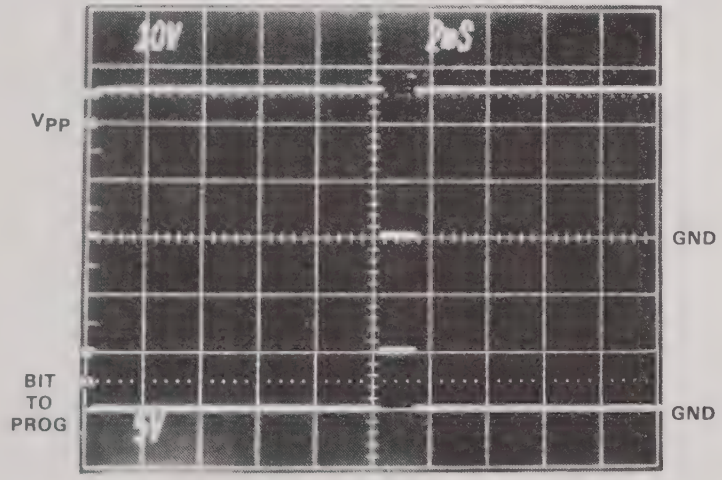
DATA I/O


10V
2
2mS
VPP
VPP
GND
TPW
PE
GND
5V

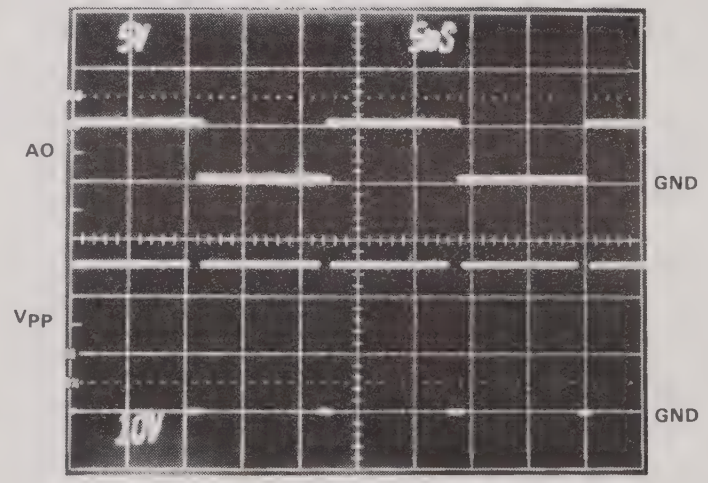
1


10V
2mS
200mS
VPP
VPPV
GND
PE
GND
5V

2


10V
2mS
VPP
GND
BIT
TO
PROG
5V
GND

3


5V
5mS
AO
GND
VPP
10V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	24.5	25.0	25.5	V	
	V_{PPV}	0.0	0.0	0.5	V	
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family BD.*
2. *Photo 1 is for Pinout 24.*
   Photo 5 is for Pinout 23.
   Photo 6 is for Pinouts 25 and 30.

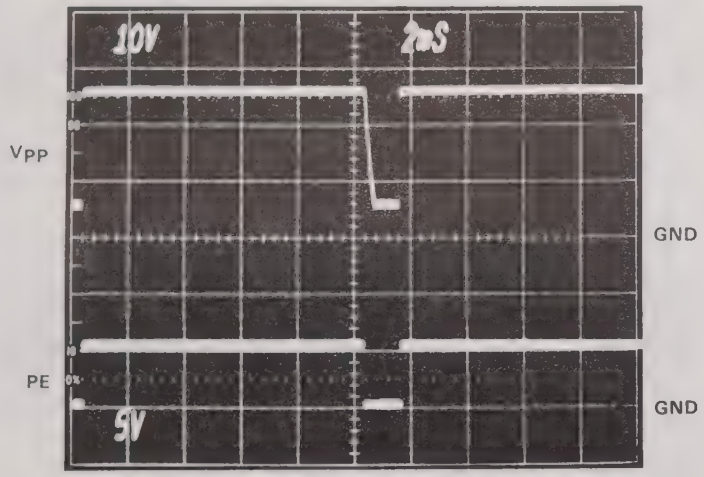
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/87

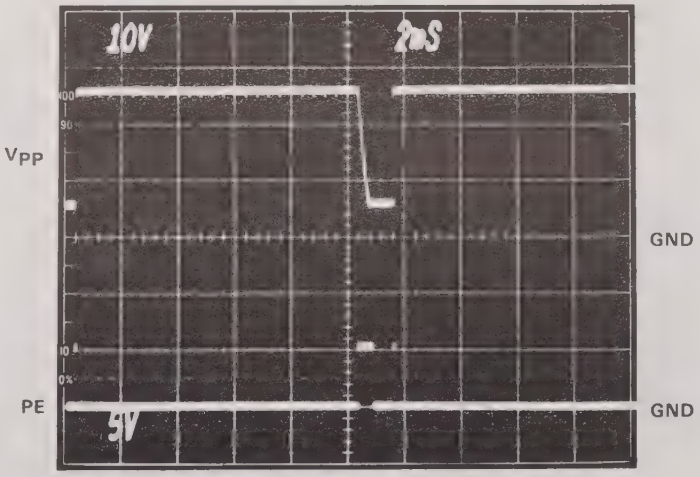
TIMING DIAGRAM

FAMILY CODES BD, BE

DATA I/O



5



6

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	0.0	0.0	0.8	V	
	V_{PPV}					N.A.
	t_{pw}	100			ns	
	t_r					N.A.
	t_{wr}	30			ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family BF.*
2. *Load pin 1 with a 330 Ω, ½-watt resistor to observe TWR in photos 1, 3 and 5.*

REVISIONS

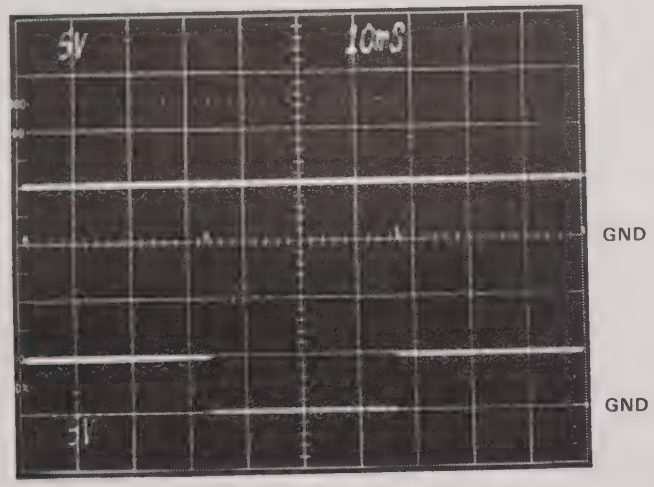
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

Sheet 1 of 2

TIMING DIAGRAM

FAMILY CODES BF, CO

DATA I/O



5

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REVISIONS

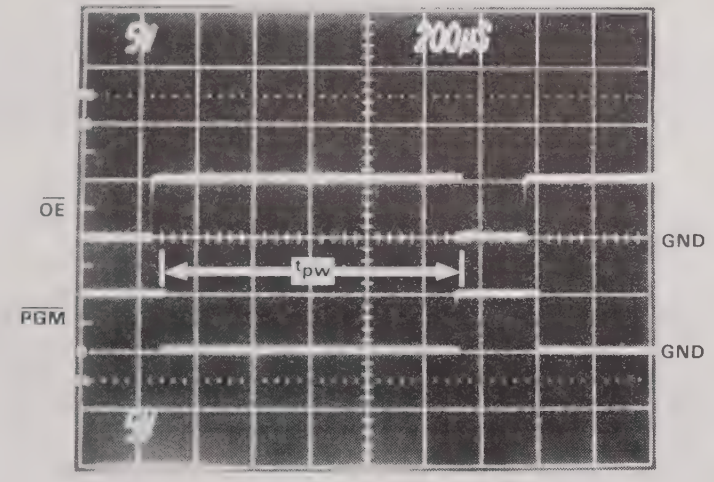
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

Sheet 2 of 2

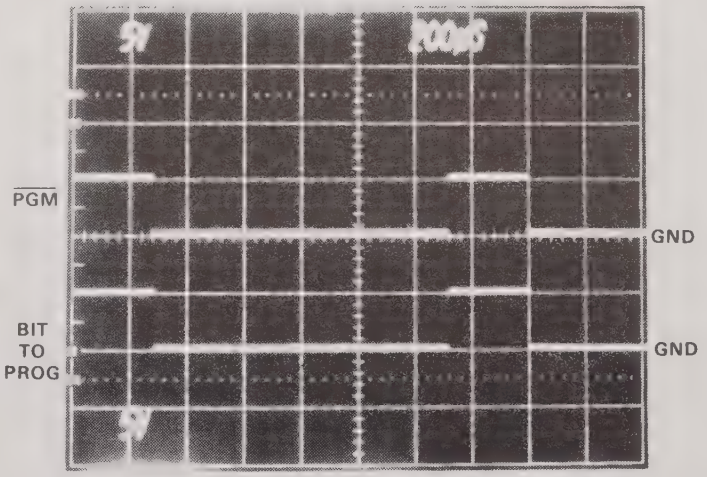
TIMING DIAGRAM

FAMILY CODES BF, CO

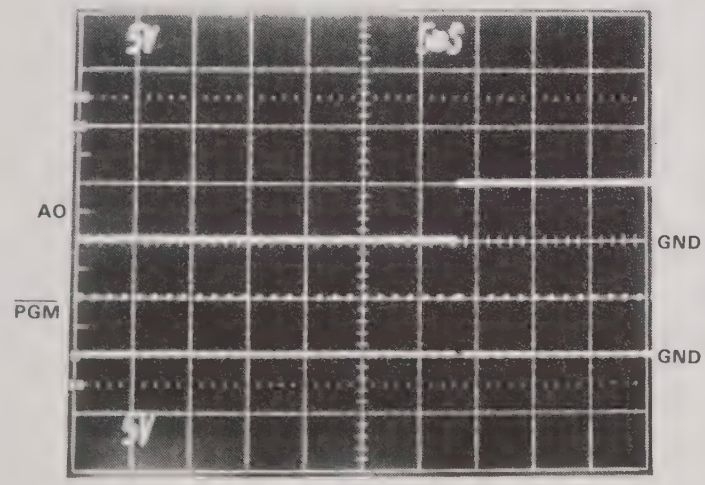
DATA I/O


5V
200μS
OE
GND
tpw
PGM
GND
5V

1


5V
200μS
PGM
GND
BIT
TO
PROG
GND
5V

2


5V
5μS
AO
GND
PGM
GND
5V

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	12.5	13.0	13.5	V	Not Shown
	V_{PPV}					
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSE	
	Overprogram		1		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. Load RAM with hex FE for Family C1.

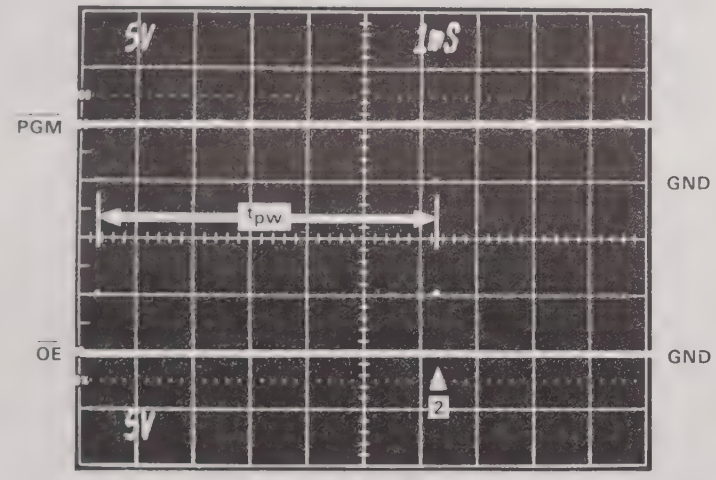
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

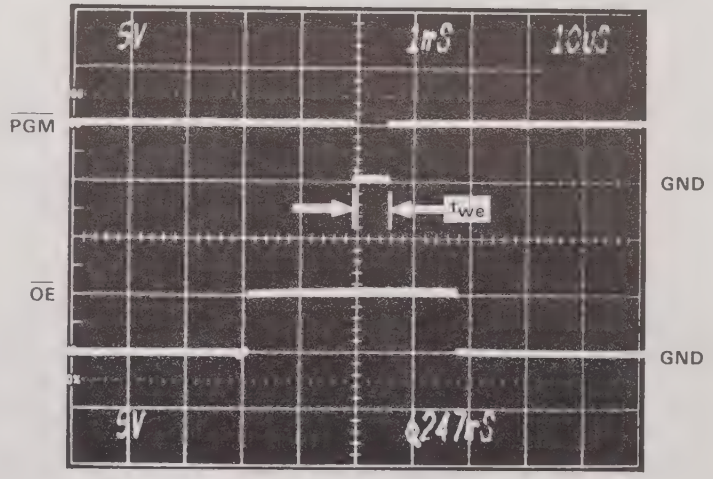
TIMING DIAGRAM

FAMILY CODES C1, C2

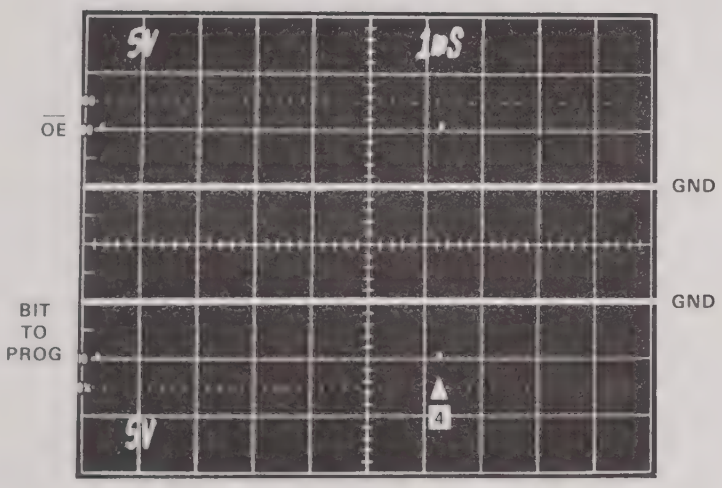
DATA I/O


5V
1mS
PGM
GND
t_{pw}
OE
GND
2
5V

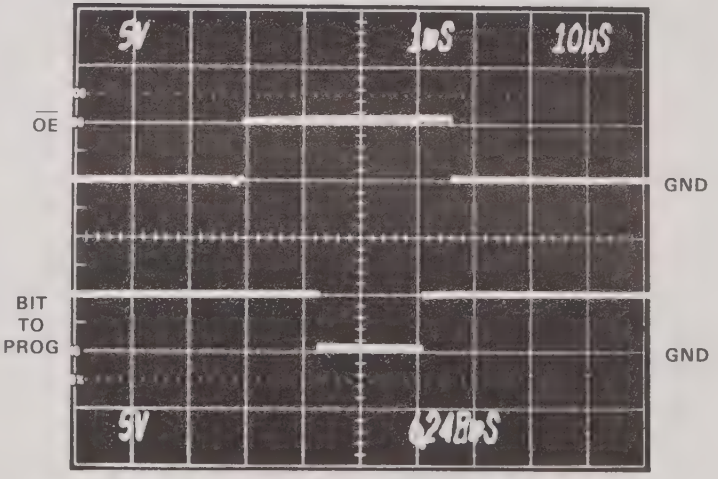
1


5V
1mS
10uS
PGM
GND
t_{we}
OE
GND
5V
247FS

2


5V
1mS
OE
GND
BIT
TO
PROG
GND
4
5V

3


5V
1mS
10uS
OE
GND
BIT
TO
PROG
GND
5V
218FS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EE}	14.5	15.0	15.5	V	
	t_{we}	150			ns	
	t_{pw}	0.1	5		ms	
	t_r					N.A.
	t_{ew}	150			ns	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.3	0.4	0.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.1	22.1	23.1	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	6.6	7.1	7.6	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family C3.*
2. *Load RAM with hex 01 for Family C4.*
3. *Photos 6 and 7 show erase pulse.*

REVISIONS

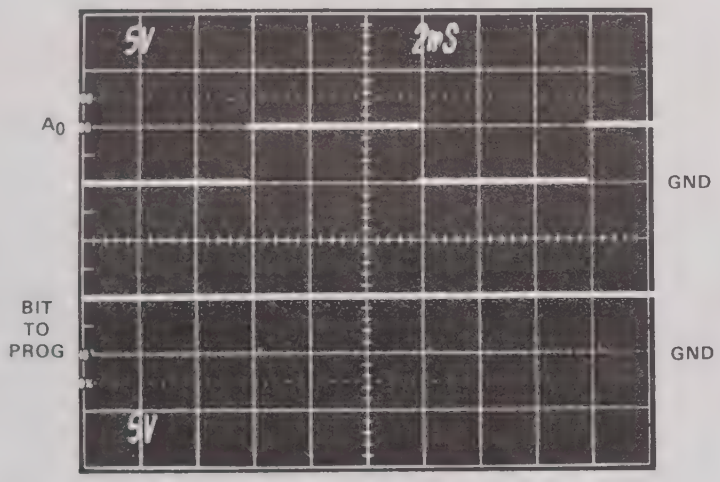
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

Sheet 1 of 2

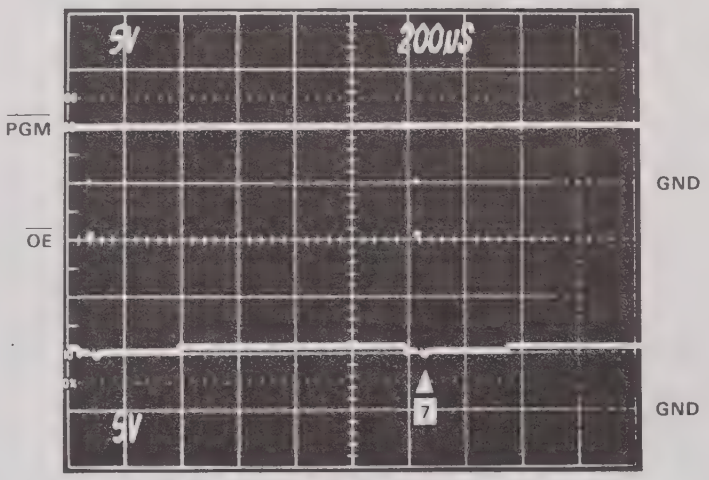
TIMING DIAGRAM

FAMILY CODES C3, C4

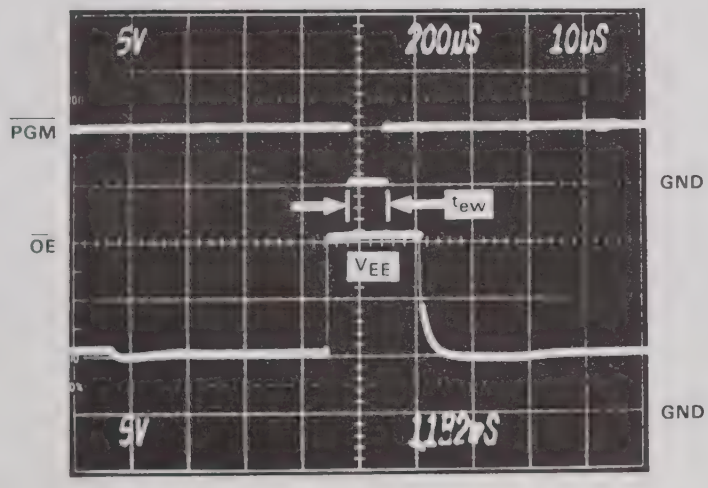
DATA I/O


5V
2mS
A_0
GND
BIT
TO
PROG
GND
5V

5


5V
200uS
PGM
GND
OE
7
GND
5V

6


5V
200uS
10uS
PGM
GND
t_{ew}
OE
V_{EE}
GND
5V

7

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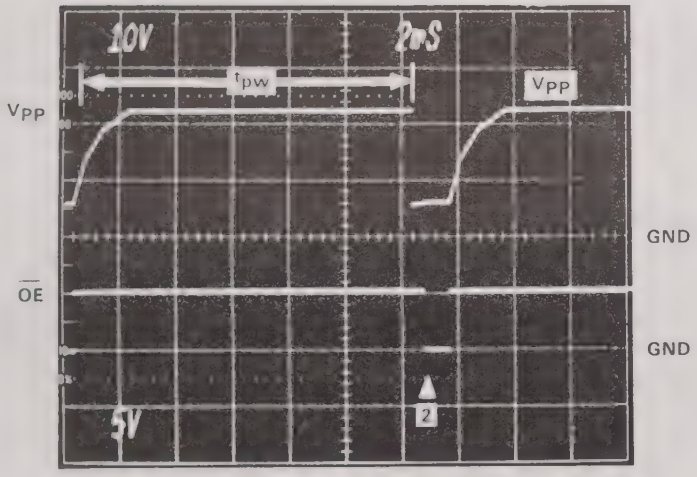
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

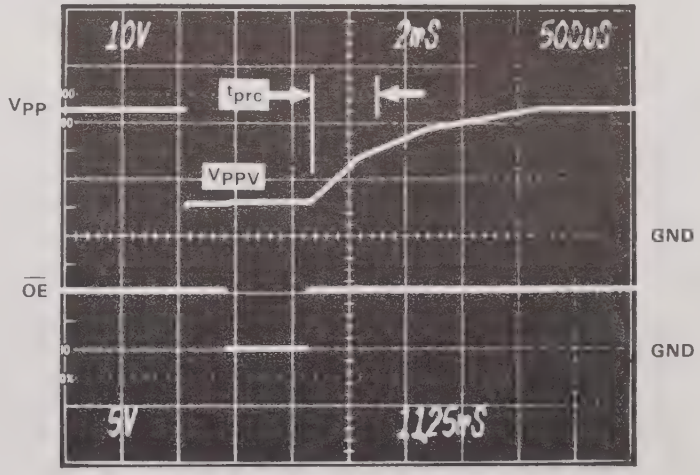
TIMING DIAGRAM

FAMILY CODES C3, C4

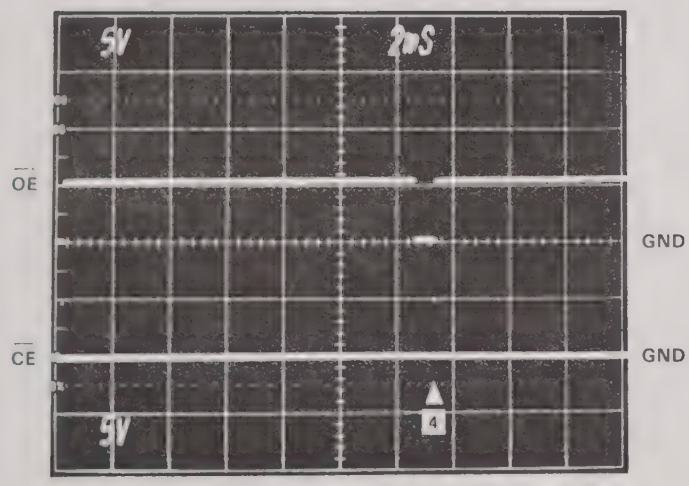
DATA I/O


10V
2mS
t_{pw}
V_{PP}
V_{PP}
GND
$\overline{OE}$
GND
5V
2

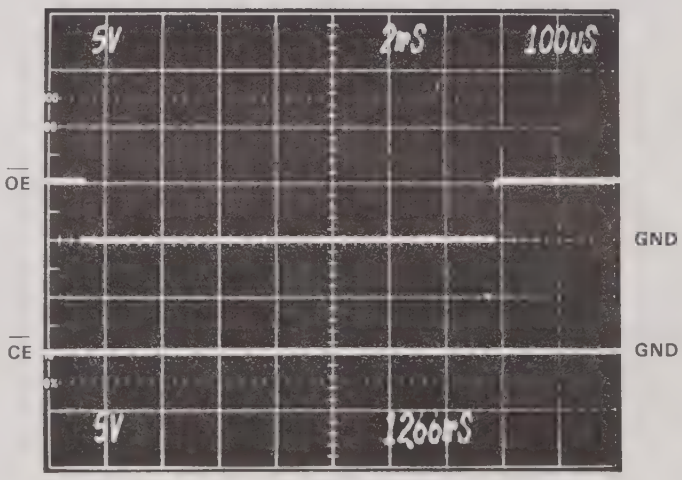
1


10V
2mS
500uS
V_{PP}
t_{prc}
V_{PPV}
GND
$\overline{OE}$
GND
5V
1125mS

2


5V
2mS
$\overline{OE}$
GND
$\overline{CE}$
GND
5V
4

3


5V
2mS
100uS
$\overline{OE}$
GND
$\overline{CE}$
GND
5V
1266mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	20.0	21.0	22.0	V	
	V_{PPV}	4.0	5.0	6.0	V	
	t_{prc}	450	600	750	μs	See note 3
	t_{pw}	9.0		15.0	ms	
	t_r					N.A.
	t_f			100	μs	
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family C7.*
2. *Load RAM with hex 01 for Family C8.*
3. *TPRC is measured from 6V to 15.5V.*

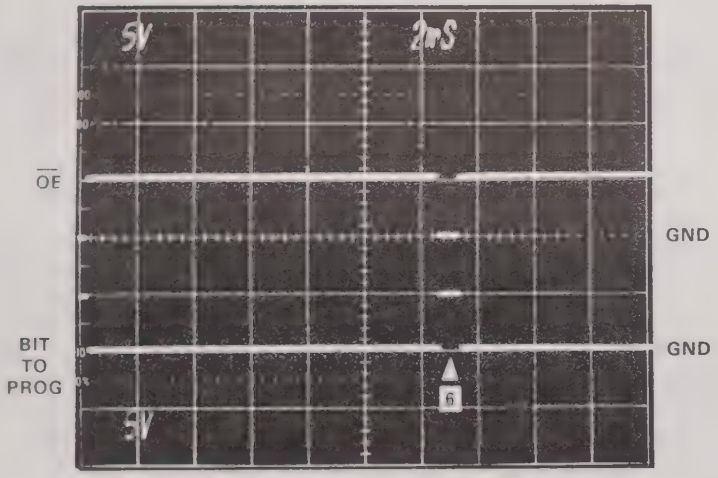
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	C78	5/84

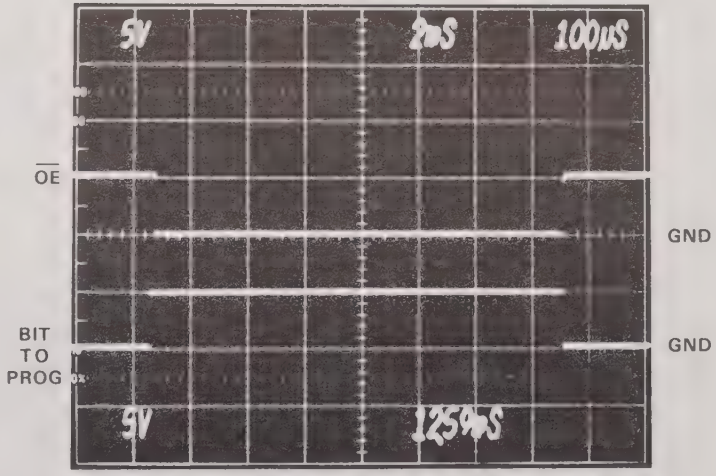
TIMING DIAGRAM

FAMILY CODES C7, C8

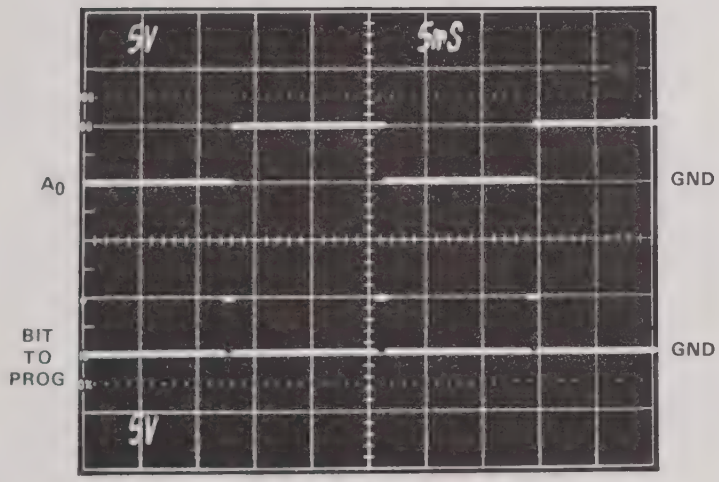
DATA I/O


5V
2mS
$\overline{OE}$
GND
BIT
TO
PROG
GND
6
5V

5


5V
2mS
100µS
$\overline{OE}$
GND
BIT
TO
PROG
GND
5V
1250µS

6


5V
5mS
A_0
GND
BIT
TO
PROG
GND
5V

7

B-211
981-0003

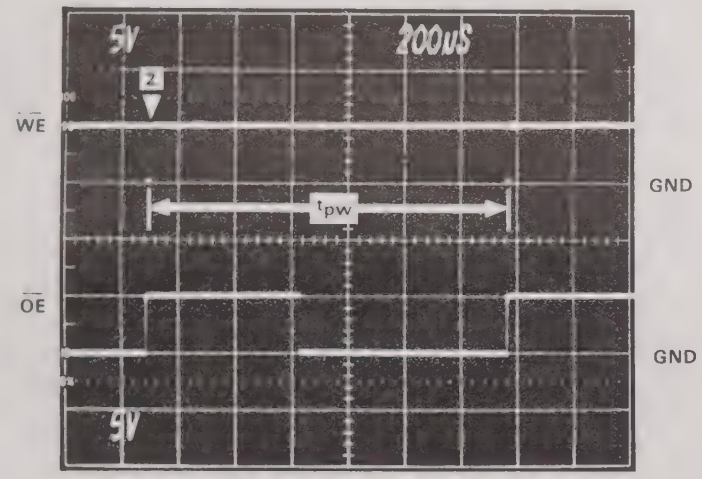
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

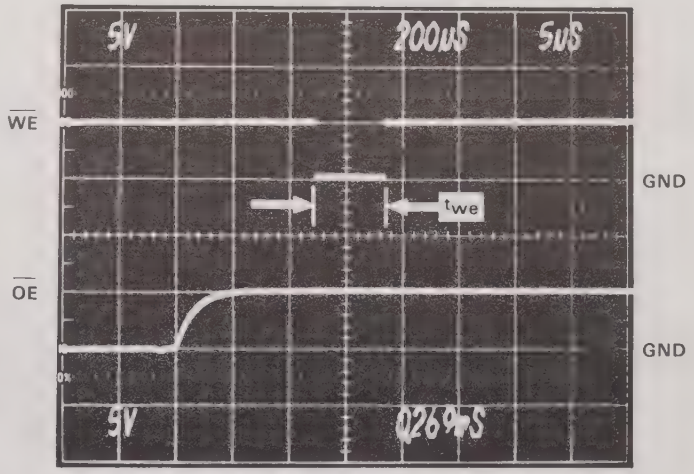
TIMING DIAGRAM

FAMILY CODES C7, C8

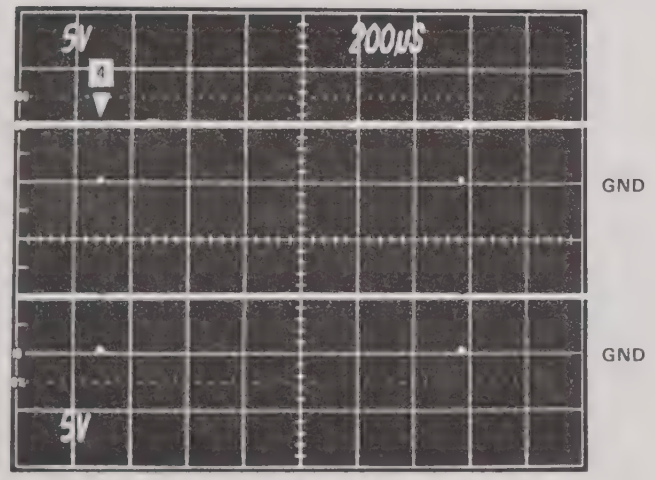
DATA I/O


5V
200uS
Z
WE
GND
tpw
OE
GND
5V

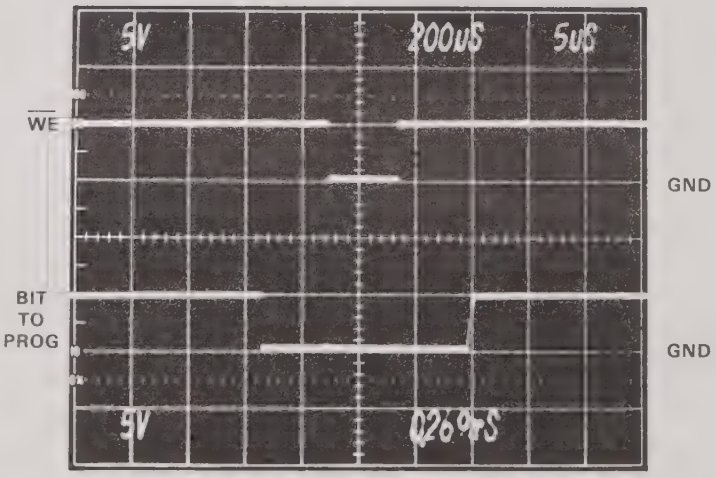
1


5V
200uS
5uS
WE
GND
twe
OE
GND
5V
0269-S

2


5V
200uS
4
WE
GND
BIT
TO
PROG
GND
5V

3


5V
200uS
5uS
WE
GND
BIT
TO
PROG
GND
5V
0269-S

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EE}	11.5	12.0	12.5	V	
	t_{we}	70			ns	
	t_{pw}	1.0		25	ms	See note 3
	t_r					N.A.
	t_{ew}	10		12	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family C9.*
2. *Load RAM with hex 01 for Family CA.*
3. *Photo 1 shows min. TPW; photo 6 shows max. TPW (load pin 1 of socket with 100Ω, ¼W resistor to observe waveform photo 6).*
4. *Photo 7 shows erase waveform.*

REVISIONS

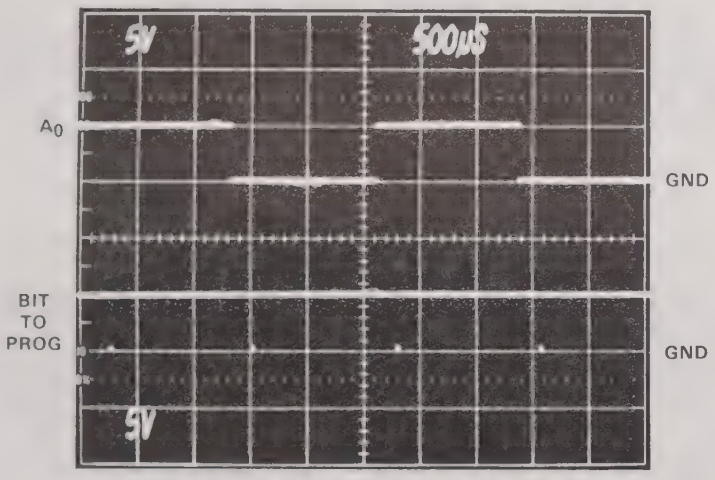
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

Sheet 1 of 2

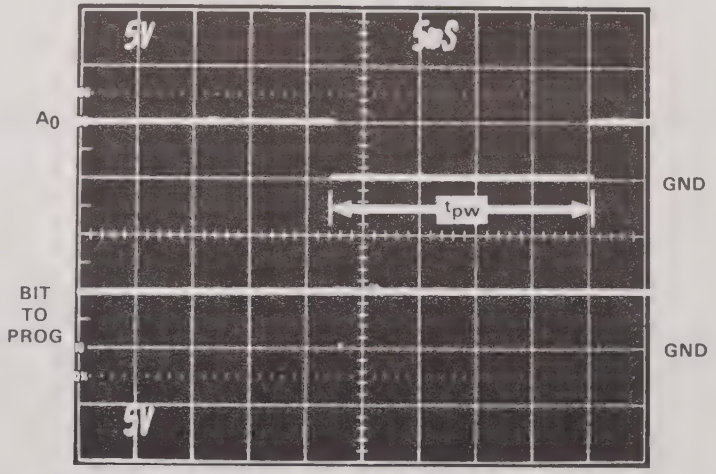
TIMING DIAGRAM

FAMILY CODES C9, CA

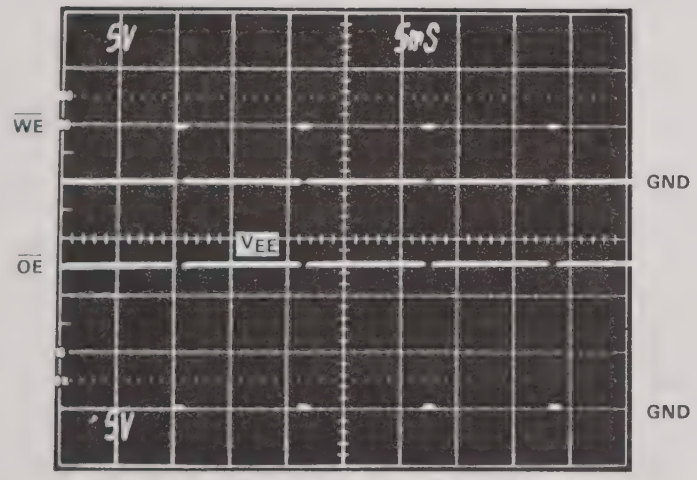
DATA I/O


5V
500µS
A0
GND
BIT
TO
PROG
GND
5V

5


5V
5µS
A0
GND
tpw
BIT
TO
PROG
GND
5V

6


5V
5µS
WE
GND
VEE
OE
GND
5V

7

B-215
981-0003

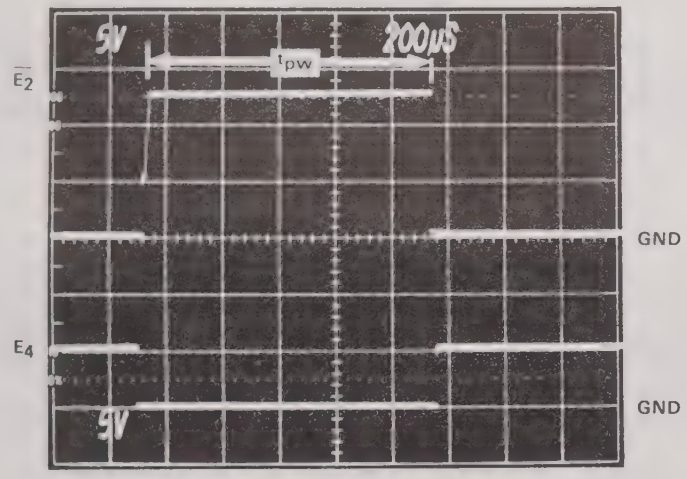
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

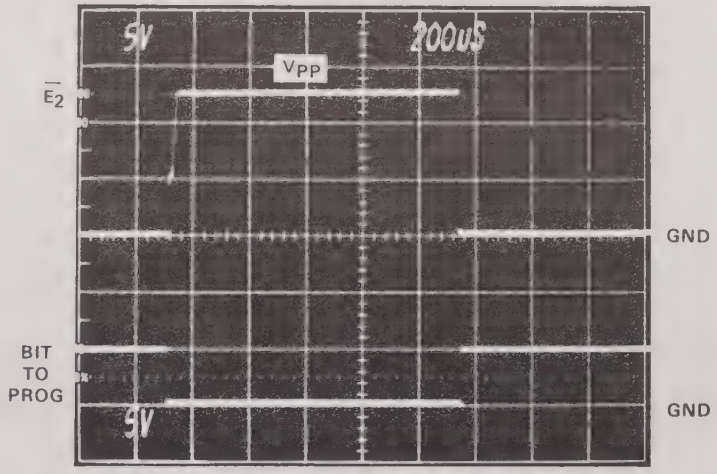
TIMING DIAGRAM

FAMILY CODES C9, CA

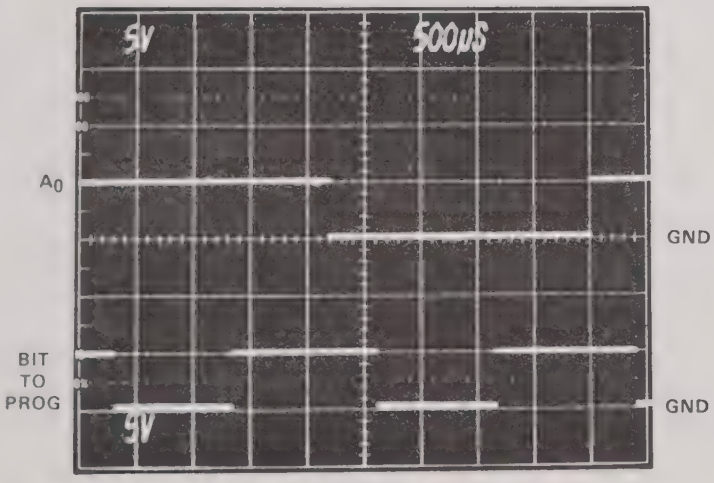
DATA I/O


5V
200uS
tpw
$\overline{E_2}$
GND
E_4
GND
5V

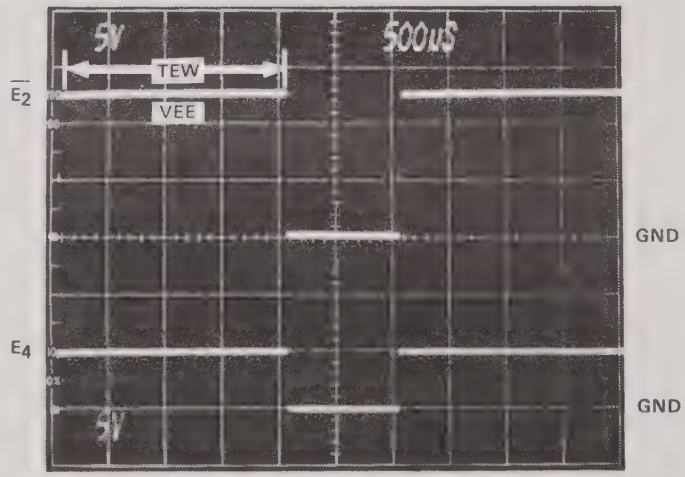
1


5V
200uS
Vpp
$\overline{E_2}$
GND
BIT
TO
PROG
GND
5V

2


5V
500uS
A_0
GND
BIT
TO
PROG
GND
5V

3


5V
500uS
TEW
VEE
$\overline{E_2}$
GND
E_4
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	11.5	12.0	12.5	V	
	V_{PPV}					N.A.
	V_{EE}	11.5	12.0	12.5	V	
	t_{pw}	1.0			ms	
	t_r					N.A.
	t_{ew}	2.0			ms	
	t_f					N.A.
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	0.7	0.8	0.9	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.5	22.5	23.5	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	1.9	2.0	2.1	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	6.2	6.7	7.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family CD.*
2. *Load RAM with hex 01 for Family CE.*
3. *Photo 4 shows erase pulse.*

REVISIONS

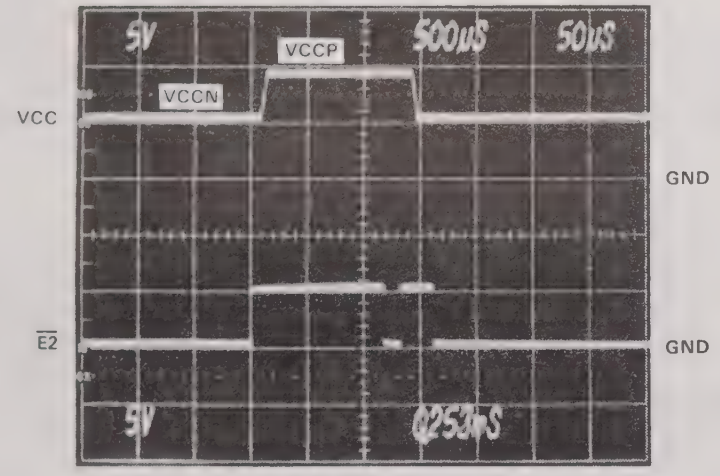
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

Sheet 1 of 1

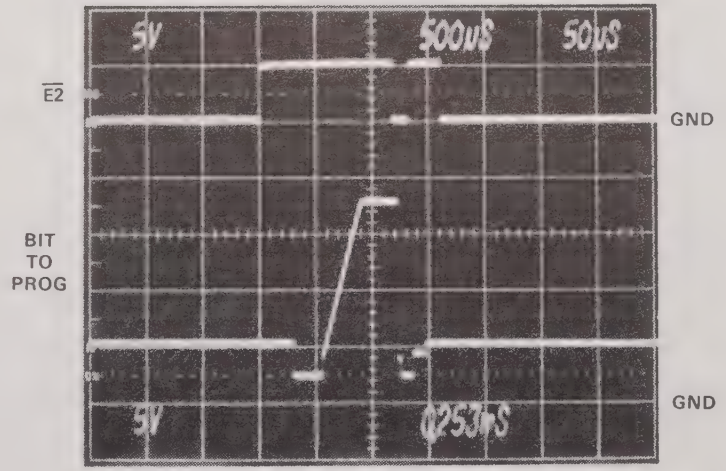
TIMING DIAGRAM

FAMILY CODES CD, CE

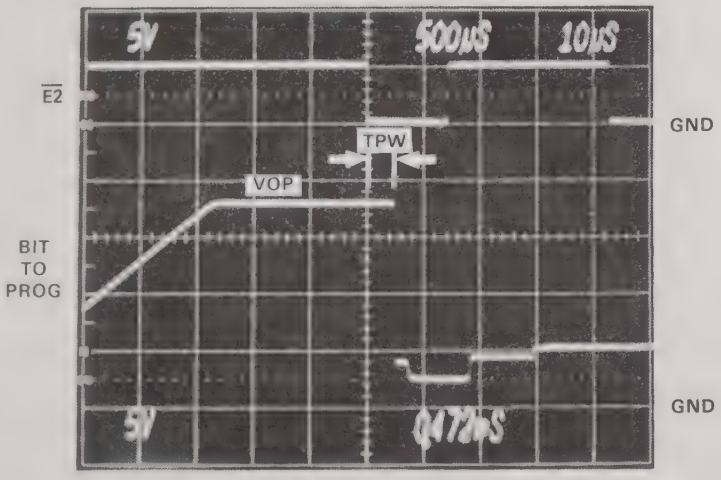
DATA I/O


5V
500uS
50uS
VCCP
VCCN
VCC
GND
E2
GND
5V
0253mS

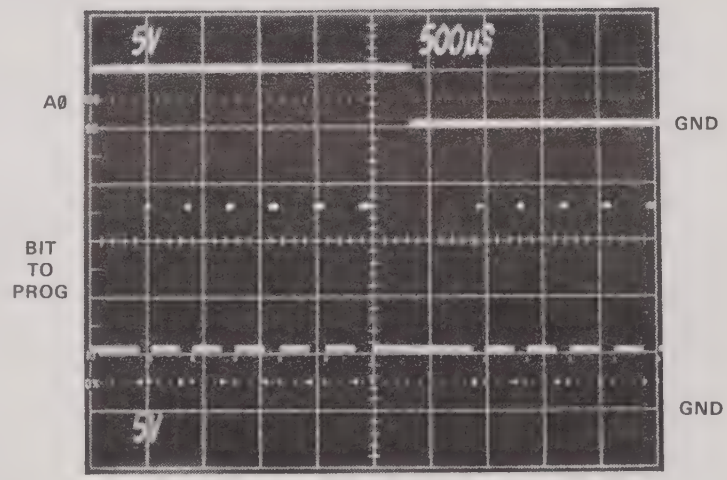
1


5V
500uS
50uS
E2
GND
BIT
TO
PROG
GND
5V
0253mS

2


5V
500uS
10uS
E2
GND
TPW
VOP
BIT
TO
PROG
GND
5V
0472mS

3


5V
500uS
A0
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	8.4	8.8	9.2	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	17.0	17.5	18.0	V	
	TPWB	4.7	5.0	5.3	μ	See Note 4
	TPWE	29.5	30.0	30.5	μ	See Note 4
	Reject		6			Pulses
	Overprogram		1			Pulse
	TOP	19.5	20.0	20.5	μ	See Note 5
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.7	0.8	0.9	V	701-1998/TP4
	High Load	23.9	24.9	25.9	V	701-1998/TP2
	Low Load	23.9	24.9	25.9	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.3	2.4	2.5	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	6.2	7.2	8.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family CF.*
2. *Load RAM with hex 01 for Family D0.*
3. *Load VCC with a 100Ω, 2-watt resistor.*
4. *TPW increases from 5 μs* to 30 μs in 5 μs increments.
5. The overprogram TPW is 20 μs. This is not shown.

REVISIONS

LTR	DESCRIPTION	P.E.	DATE

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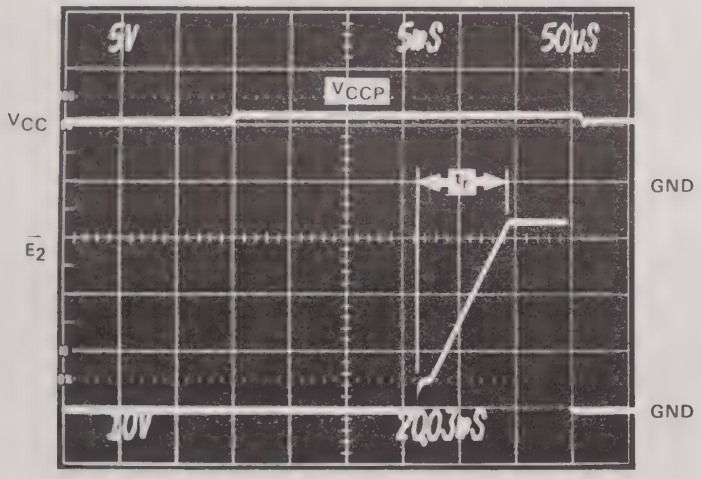
TIMING DIAGRAM

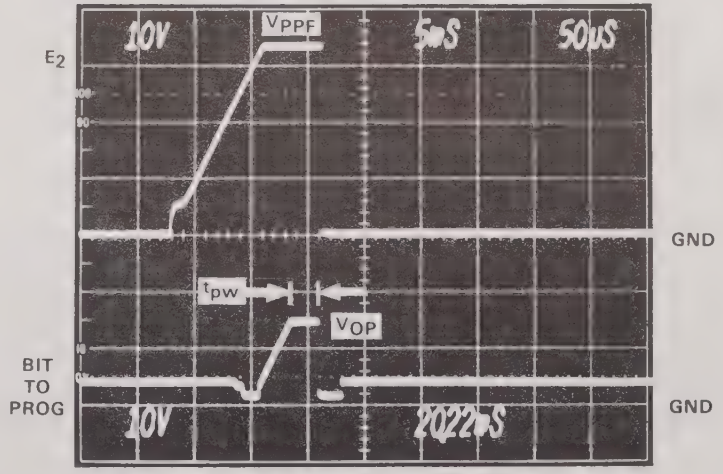
FAMILY CODES CF, D0

DATA I/O

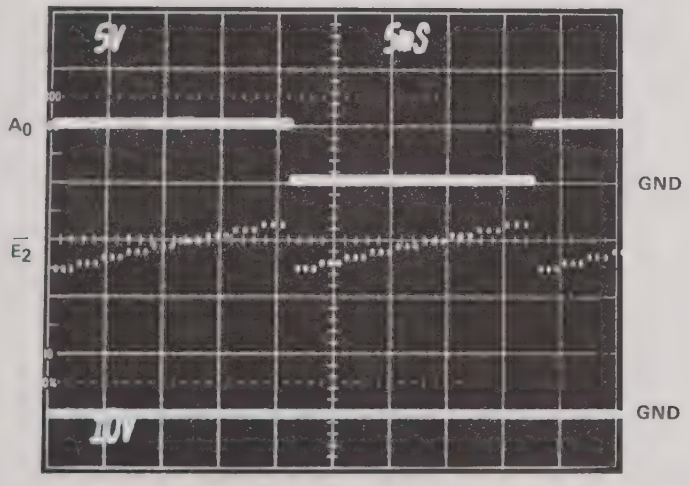
0526/1282


5V
5mS
50uS
V_{CCP}
V_{CC}
t_r
$\overline{E_2}$
GND
GND
10V
2003mS

1


10V
V_{PPF}
5mS
50uS
E_2
GND
t_{pw}
V_{OP}
BIT
TO
PROG
GND
10V
2022mS

2


5V
5mS
A_0
GND
$\overline{E_2}$
GND
10V

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.25	5.5	5.75	V	
	V_{OP}	14.5	15.0	15.5	V	
	V_{PPS}	24.0	25.0	26.0	V	See note 3
	V_{PPF}	32.0	33.0	34.0	V	See note 3
	t_{pw}	10.0		40	μs	
	t_r	53	66	88	μs	See note 4
	t_f					N.A.
	Reject		27		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.1	4.2	4.3	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	17.3	18.3	19.3	V	701-1998/TP2
	LOW LOAD	17.3	18.3	19.3	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	2.9	3.0	3.1	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	5.2	5.7	6.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family D1.*
2. *Load RAM with hex 01 for Family D2.*
3. *V_{PP} starts at 25V and increments to 33V in 1-volt steps with 3 pulses per step.*
4. *TR is measured 10% to 90% of greatest amplitude $\overline{E_2}$ pulse.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

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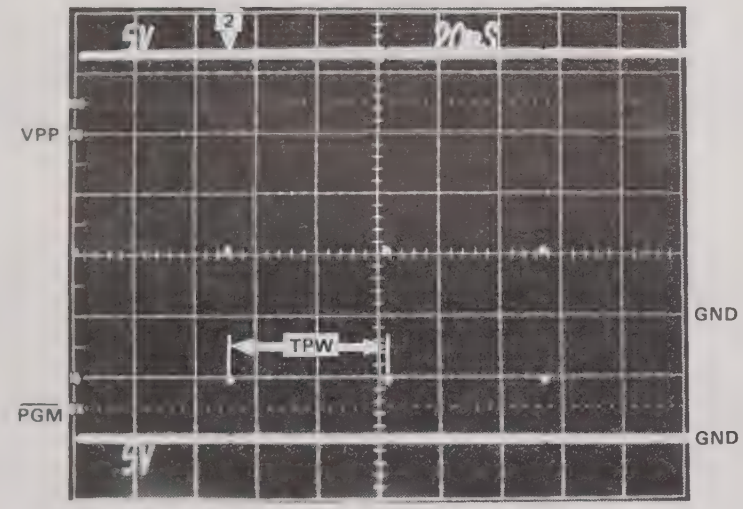
TIMING DIAGRAM

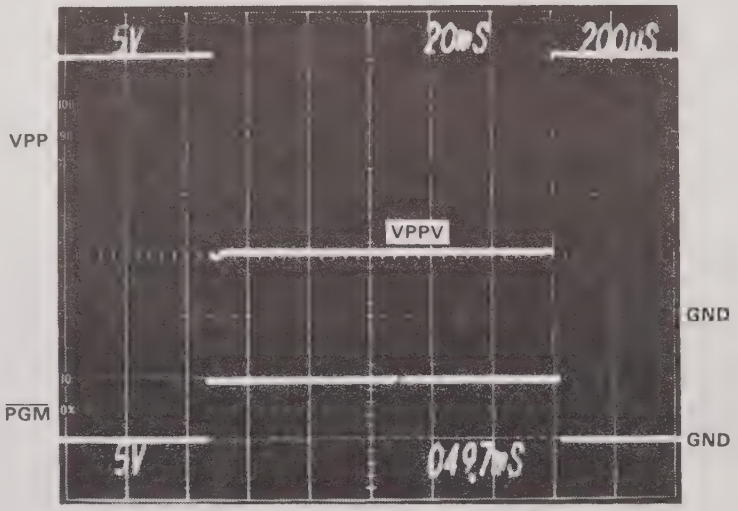
FAMILY CODES D1, D2

DATA I/O

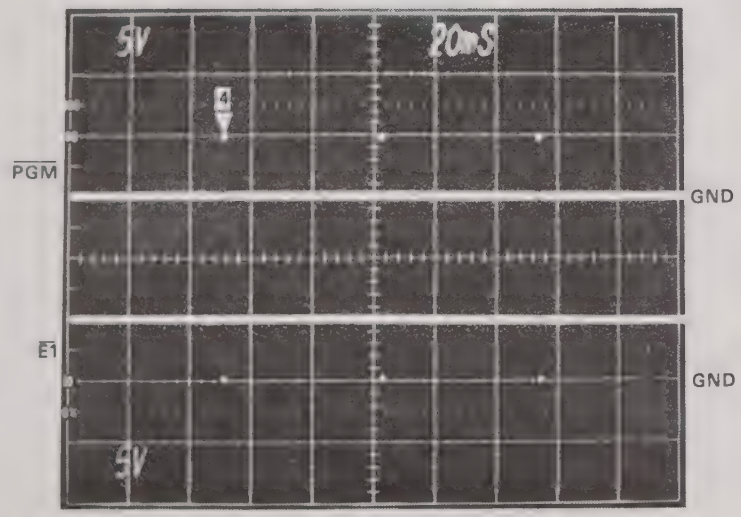
0526/1282


5V
2
20mS
VPP
TPW
GND
PGM
GND
5V

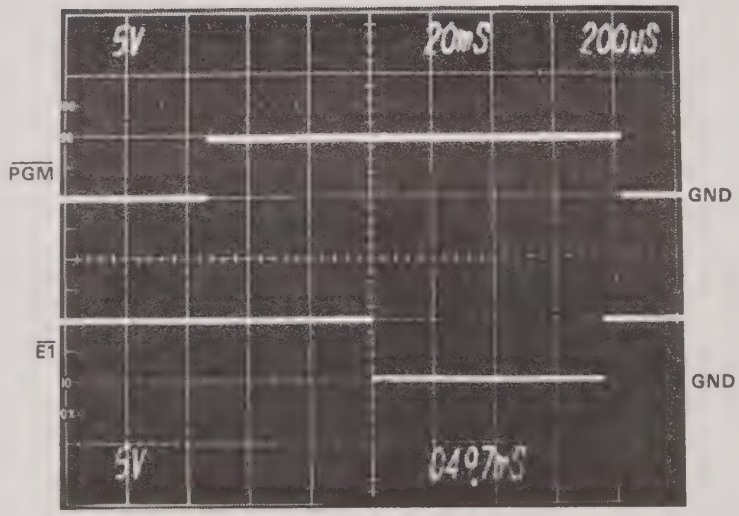
1


5V
20mS
200uS
VPP
VPPV
GND
PGM
GND
5V
049.7mS

2


5V
20mS
4
PGM
GND
E1
GND
5V

3


5V
20mS
200uS
PGM
GND
E1
GND
5V
049.7mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					N.A.
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					N.A.
	TF					N.A.
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 53.*
2. *Load RAM with hex 01 for Family 54 and bit-to-prog waveform becomes bit-no-prog waveform.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

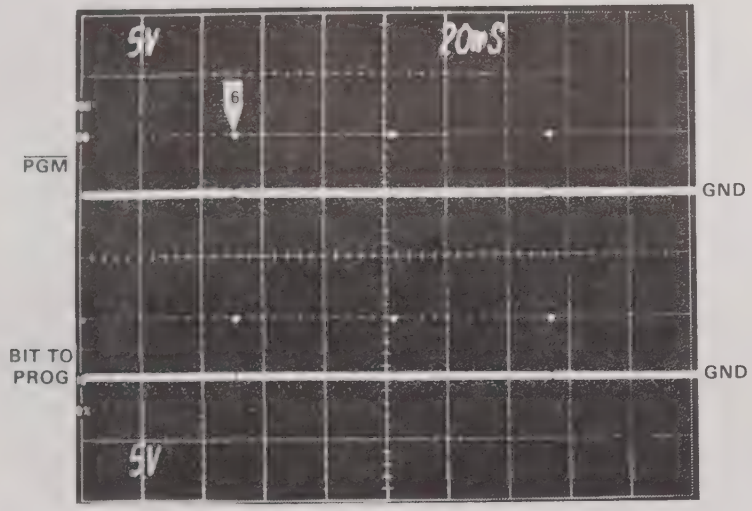
Sheet 1 of 2

TIMING DIAGRAM

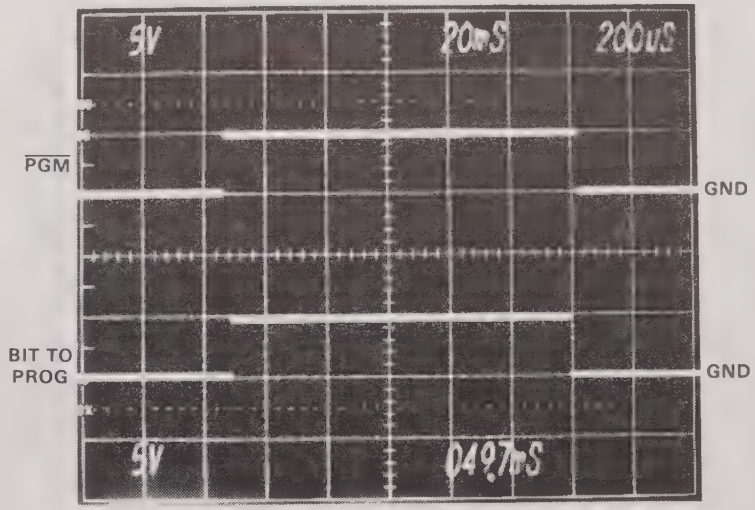
FAMILY CODES D5, D6

DATA I/O

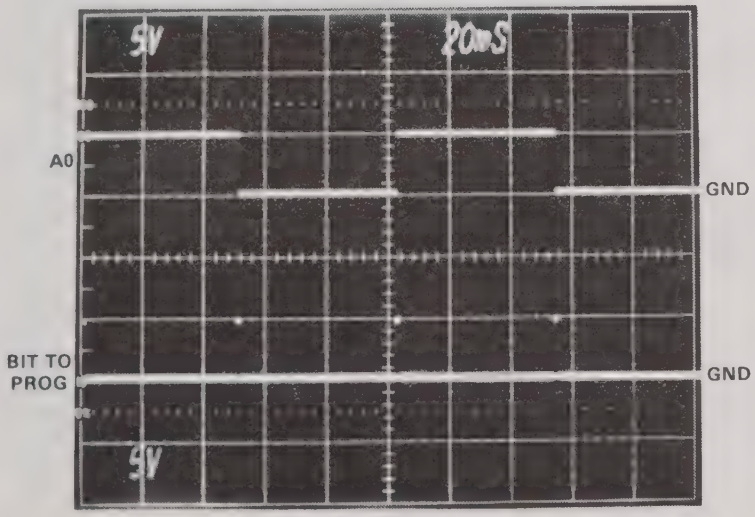
0526/1282


5V
20mS
6
PGM
GND
BIT TO PROG
GND
5V

5


5V
20mS
200uS
PGM
GND
BIT TO PROG
GND
5V
049.7mS

6


5V
20mS
A0
GND
BIT TO PROG
GND
5V

7

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/14

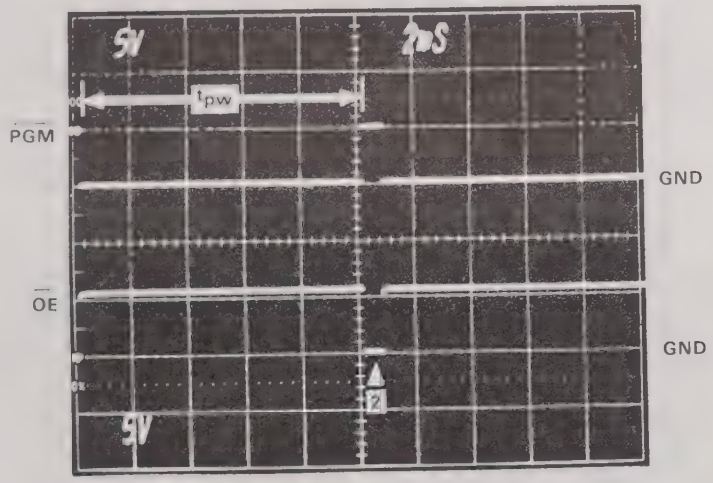
Sheet 2 of 2

TIMING DIAGRAM

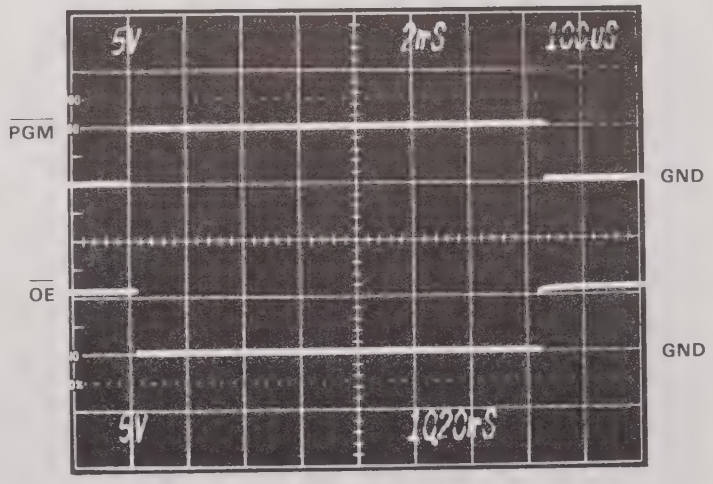
FAMILY CODES D5, D6

DATA I/O

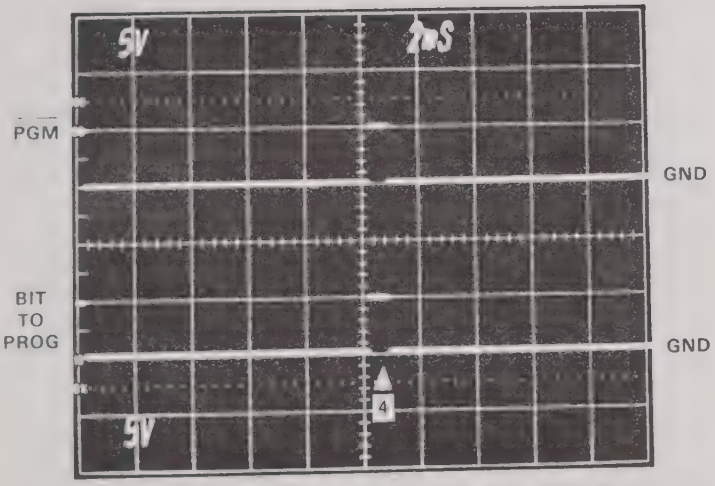
0526/1282


5V
2mS
t_{pw}
PGM
GND
OE
GND
2
5V

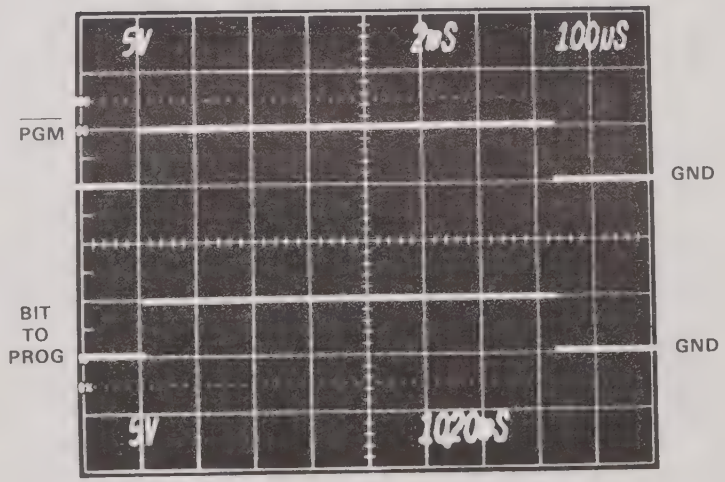
1


5V
2mS
100uS
PGM
GND
OE
GND
5V

2


5V
2mS
PGM
GND
BIT
TO
PROG
GND
4
5V

3


5V
2mS
100uS
PGM
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_{ew}	95	100	105	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.4	22.4	23.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	7.4	7.9	8.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family D7.*
2. *Load RAM with hex 01 for Family D8.*
3. *Photo 6 shows chip erase.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

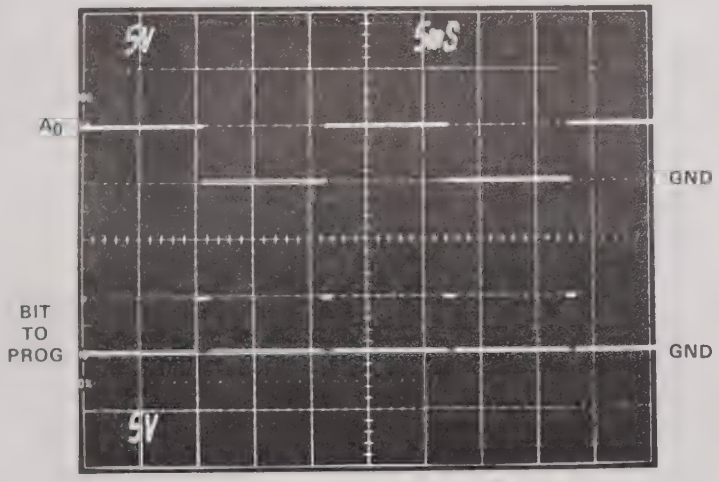
Sheet 1 of 2

TIMING DIAGRAM

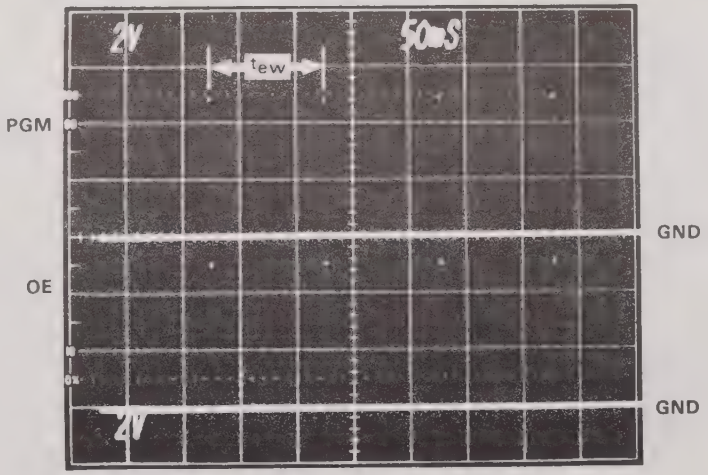
FAMILY CODES D7, D8

DATA I/O

0526/1282



5



6

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

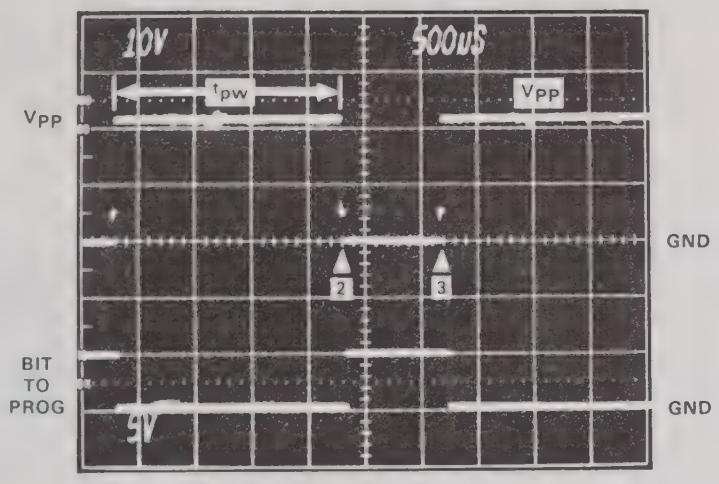
Sheet 2 of 2

TIMING DIAGRAM

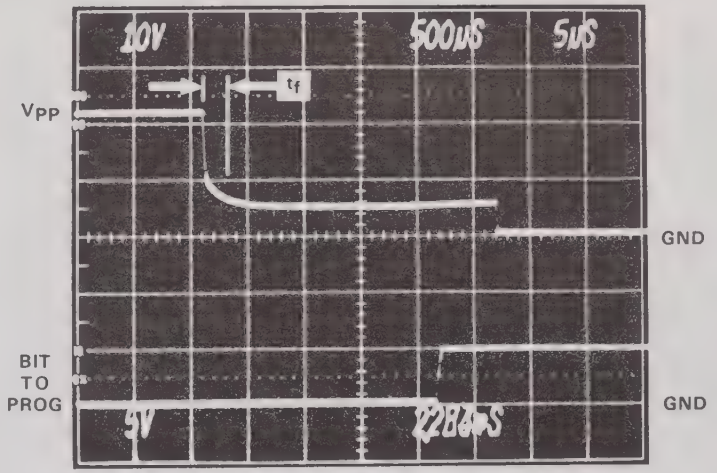
FAMILY CODES D7, D8

DATA I/O

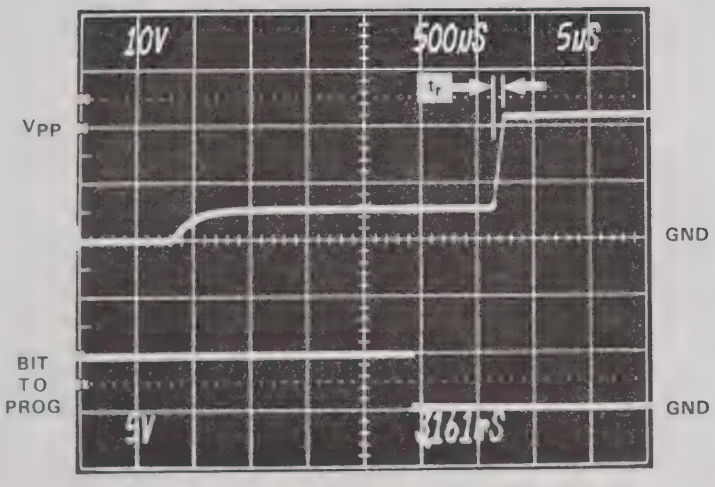
0526/1282


10V
500uS
t_{pw}
V_{PP}
V_{PP}
GND
2
3
BIT
TO
PROG
GND
9V

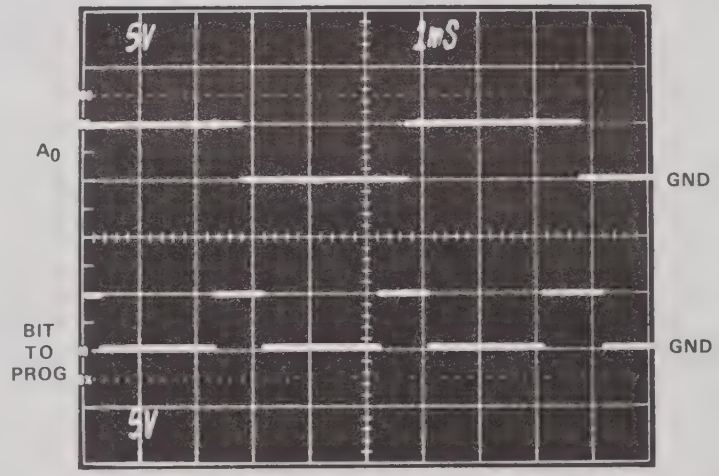
1


10V
500uS
5uS
t_f
V_{PP}
GND
BIT
TO
PROG
GND
9V

2


10V
500uS
5uS
t_r
V_{PP}
GND
BIT
TO
PROG
GND
9V

3


9V
1mS
A_0
GND
BIT
TO
PROG
GND
9V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	20.5	21.0	21.5	V	
	V_{PP}					N.A.
	V_{PPV}					
	t_{pw}	1.9	2.0	2.1	ms	
	t_r	0.5		2.0	μs	
	t_f	0.5		5.0	μs	
	Reject		20		PASSES	
	Overprogram		5		PASSES	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.4	0.5	0.6	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.2	22.2	23.2	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	6.6	7.1	7.6	V	701-1998/TP3

NOTES

1. Load RAM with hex FE for Family D9
2. Load RAM with hex 01 for Family DA.

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

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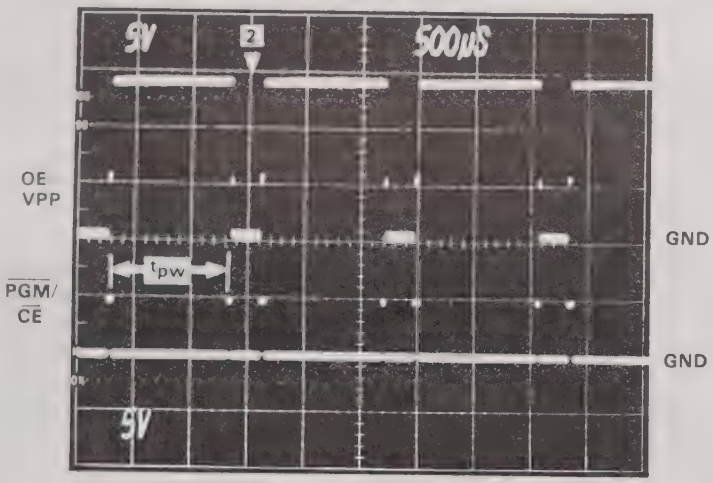
TIMING DIAGRAM

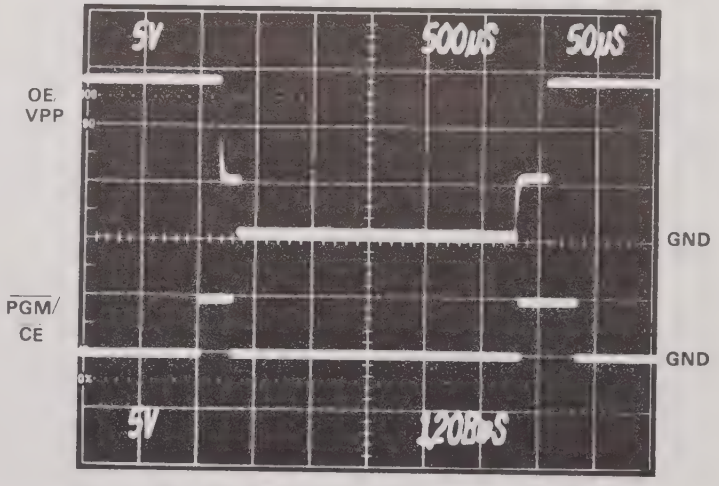
FAMILY CODES D9, DA

DATA I/O

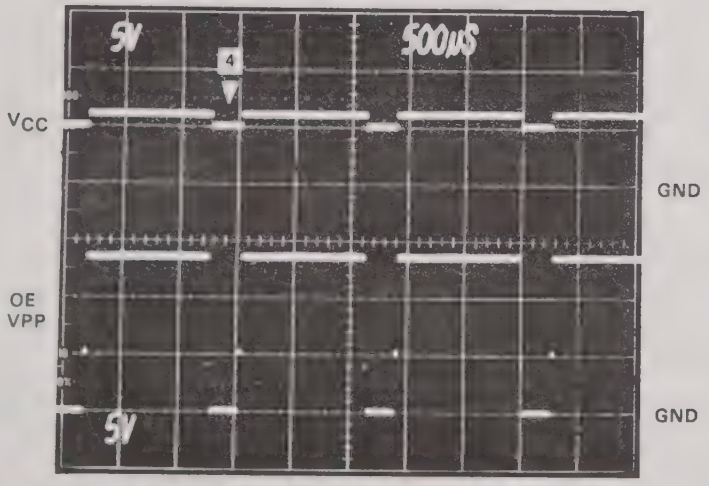
0526/1282


5V
2
500µS
OE
VPP
GND
t_{pw}
PGM/
CE
GND
5V

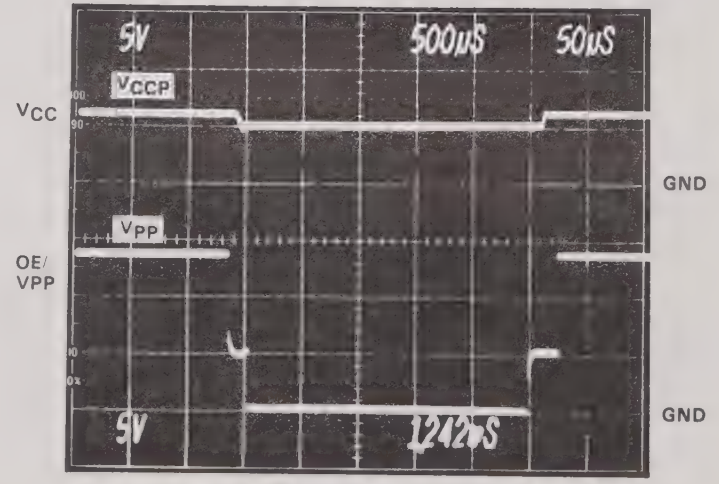
1


5V
500µS
50µS
OE
VPP
GND
PGM/
CE
GND
5V

2


5V
4
500µS
VCC
GND
OE
VPP
GND
5V

3


5V
500µS
50µS
VCCP
VCC
GND
VPP
OE/
VPP
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	
	V_{OP}					N.A.
	V_{PP}	12.5	13.0	13.5	V	
	V_{PPV}					N.A.
	t_{pw}	0.95	1	1.05	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSES	
	Overprogram		1		PULSES	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family DD.*
2. *Load RAM with hex 01 for Family DE.*

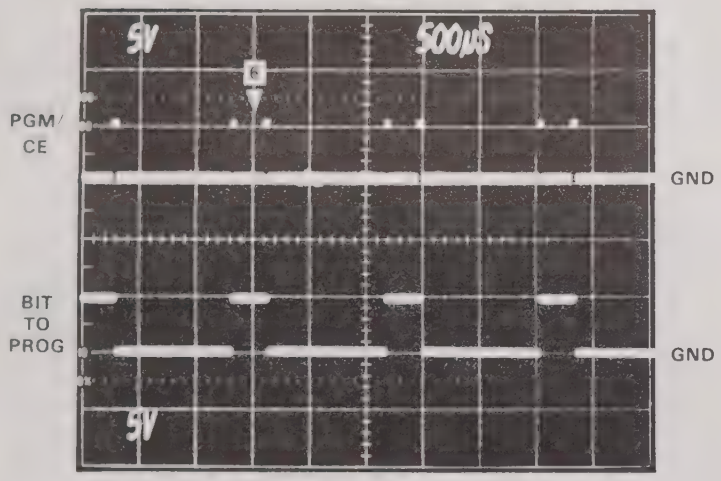
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/24

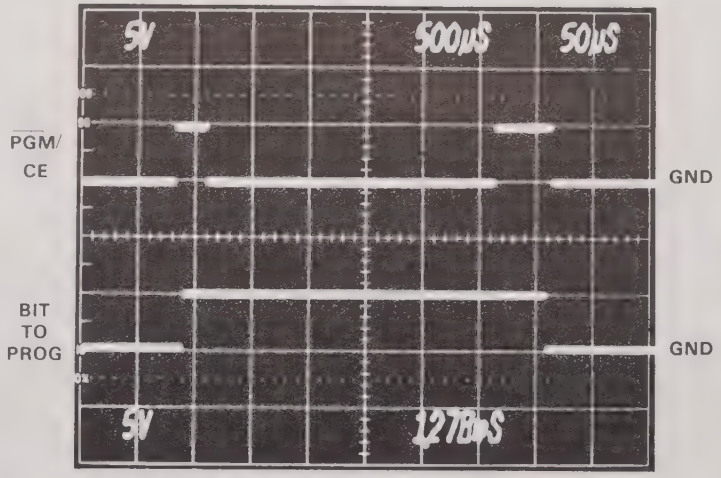
TIMING DIAGRAM

FAMILY CODES DD, DE

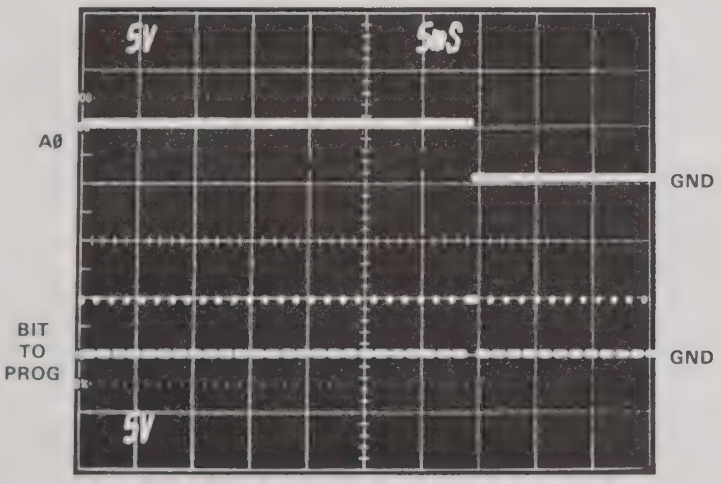
DATA I/O


5V
500µS
PGM/
CE
GND
BIT
TO
PROG
GND
5V

5


5V
500µS
50µS
PGM/
CE
GND
BIT
TO
PROG
GND
5V

6


5V
A0
GND
BIT
TO
PROG
GND
5V

7

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REVISIONS

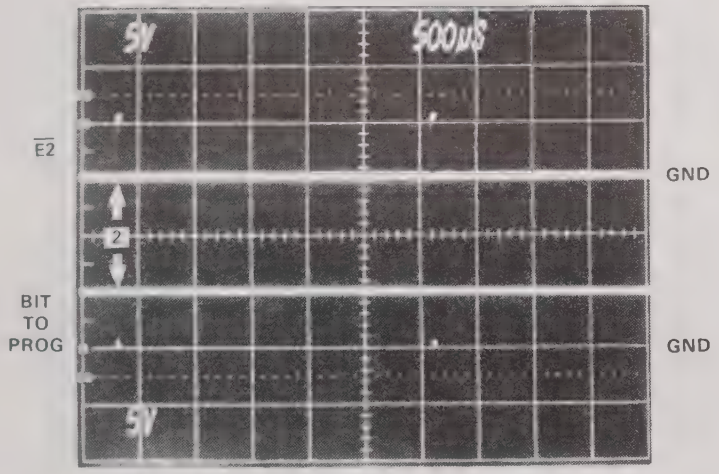
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/24

Sheet 2 of 2

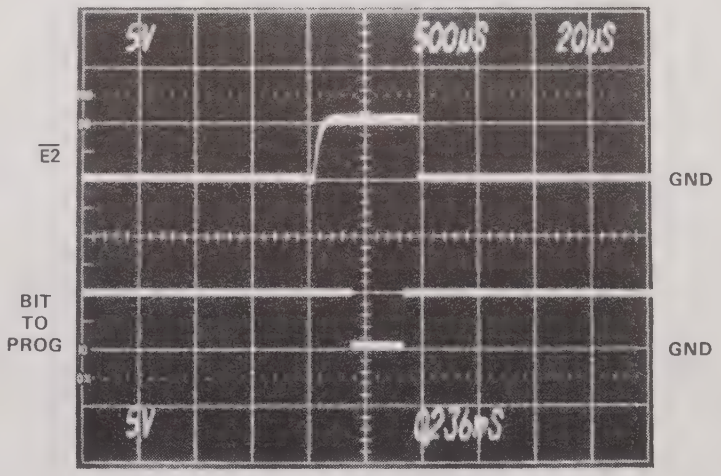
TIMING DIAGRAM

FAMILY CODES DD, DE

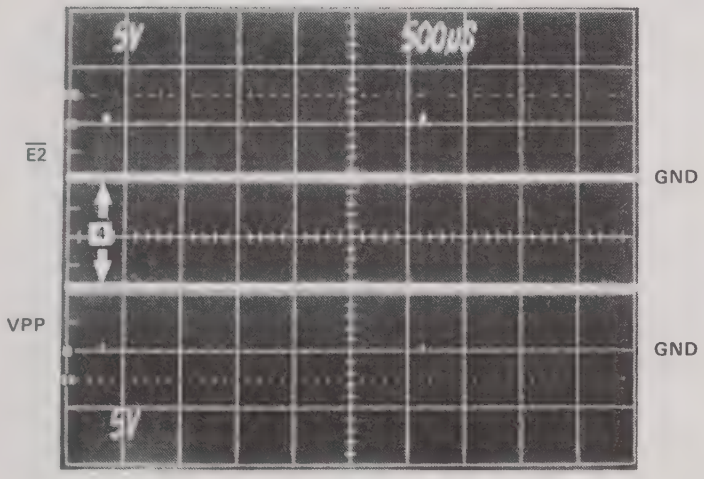
DATA I/O


5V
500µS
E2
GND
2
BIT
TO
PROG
GND
5V

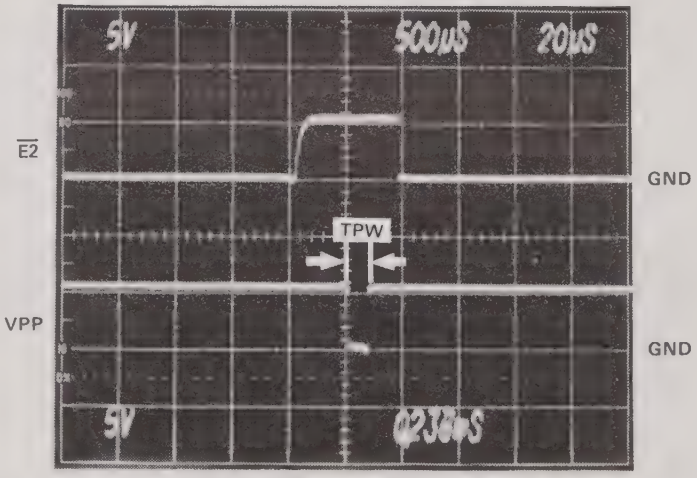
1


5V
500µS
20µS
E2
GND
BIT
TO
PROG
GND
5V

2


5V
500µS
E2
GND
4
VPP
GND
5V

3


5V
500µS
20µS
E2
GND
TPW
VPP
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VEP	20.5	21.0	21.5	V	
	VEE	11.5	12.0	12.5	V	
	TPW	150			ns	
	TEW	9.0		15.0	ms	
	Reject		1		Pulse	
	Overprogram		0		Pulses	
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.3	0.4	0.5	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	21.1	22.1	23.1	V	701-1998/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.3	2.4	2.5	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	6.6	7.1	7.6	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family DF.*
2. *Load RAM with hex 01 for Family E0.*
3. *Photo 6 shows erase pulse.*

REVISIONS

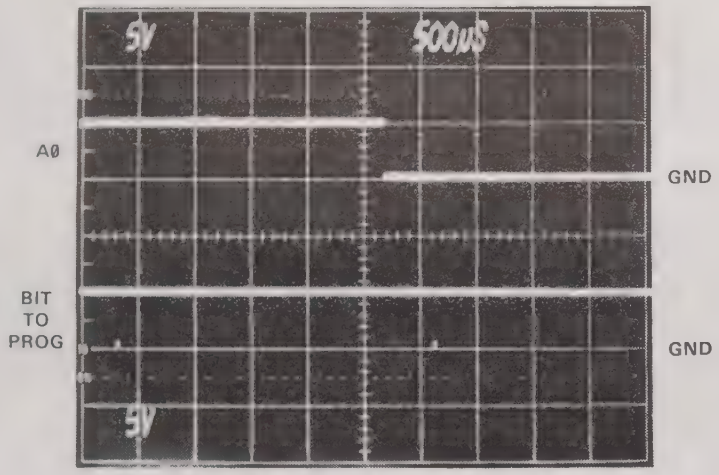
LTR	DESCRIPTION	P.E.	DATE

Sheet 1 of 2

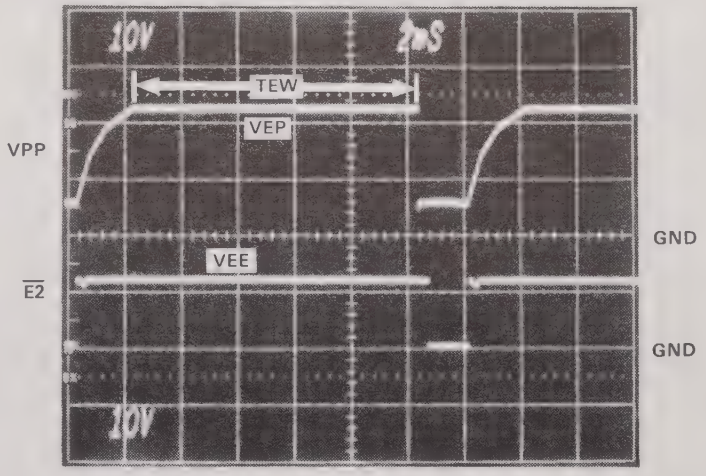
TIMING DIAGRAM

FAMILY CODES DF, E0

DATA I/O


5V
500uS
A0
GND
BIT
TO
PROG
GND
5V

5


10V
2mS
TEW
VEP
VPP
GND
VEE
$\overline{E2}$
GND
10V

6

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LTR	DESCRIPTION	P.E.	DATE

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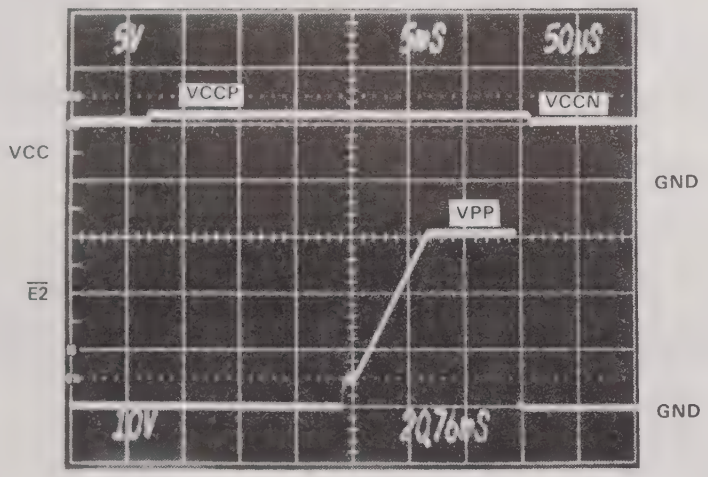
TIMING DIAGRAM

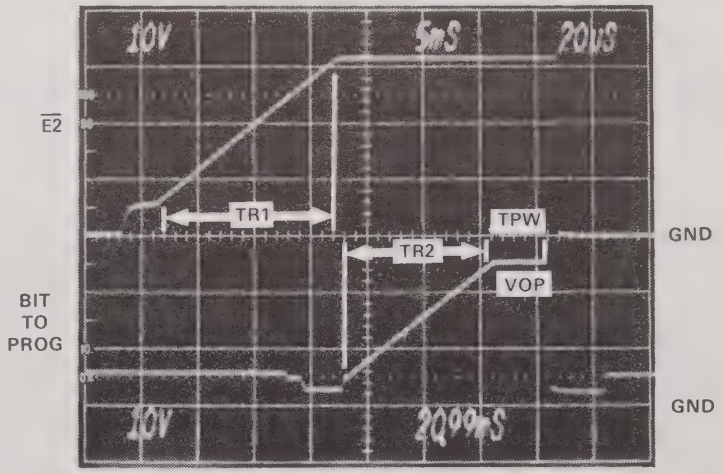
FAMILY CODES DF, E0

DATA I/O

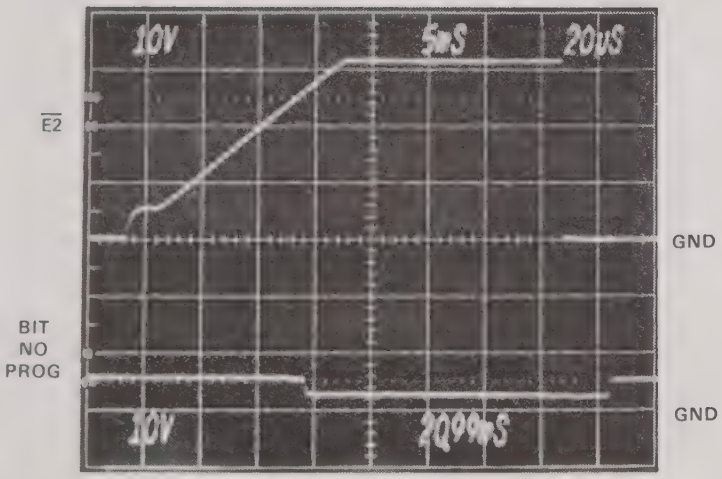
0526/1282


5V
5mS
50uS
VCCP
VCCN
VCC
GND
VPP
E2
GND
10V
20.76mS

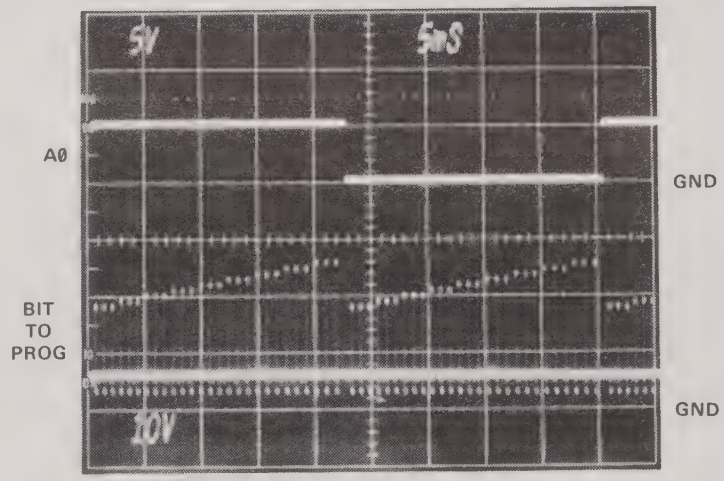
1


10V
5mS
20uS
E2
TR1
TPW
GND
TR2
VOP
BIT
TO
PROG
GND
10V
20.00mS

2


10V
5mS
20uS
E2
GND
BIT
NO
PROG
GND
10V
20.00mS

3


5V
5mS
A0
GND
BIT
TO
PROG
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.3	5.5	5.7	V	
	VCCN	4.75	5.0	5.25	V	
	VOPB	16.5	17.0	17.5	V	See Note 3
	VOPE	24.5	25.0	25.5	V	See Note 3
	VPPB	22.5	23.0	23.5	V	See Note 3
	VPPE	30.5	31.0	31.5	V	See Note 3
	TPW	10.0		40.0	μs	See Note 4
	TR1	50	63	82	μs	See Note 5
	TR2	40	50	66	μs	See Note 5
	Reject		27		Pulses	
	Overprogram		0		Pulses	
1ST PASS	VCC	4.1	4.2	4.3	V	
VERIFY	VREF	0.8	0.9	1.0	V	701-1998/TP4
	High Load	17.3	18.3	19.3	V	701-1998/TP2
	Low Load	17.3	18.3	19.3	V	701-1998/TP3
2ND PASS	VCC	5.9	6.0	6.1	V	
VERIFY	VREF	2.9	3.0	3.1	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.7	5.7	6.7	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family E5.*
2. *Load RAM with hex 01 for Family E6.*
3. *These levels increment in 1-volt steps.*
4. *This is measured at the 90% level, and all nine pulse levels must meet this spec.*
5. *This is measured from 10% to 90% of the tallest pulse.*

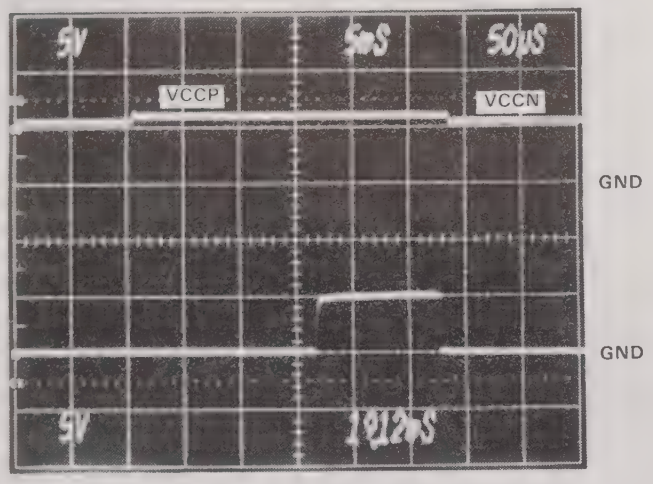
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

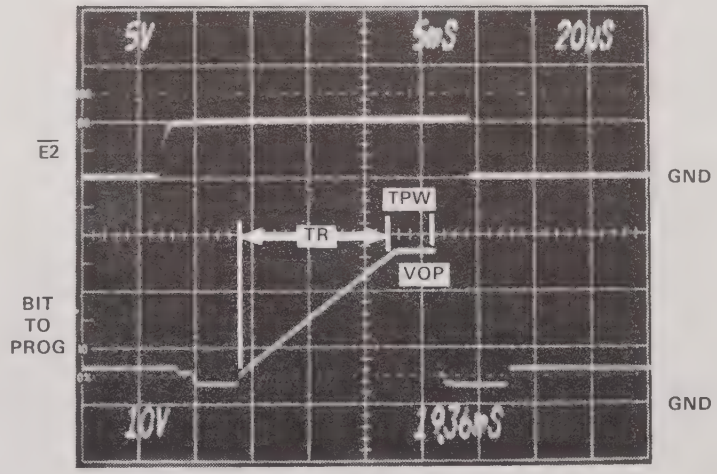
TIMING DIAGRAM

FAMILY CODES E5, E6

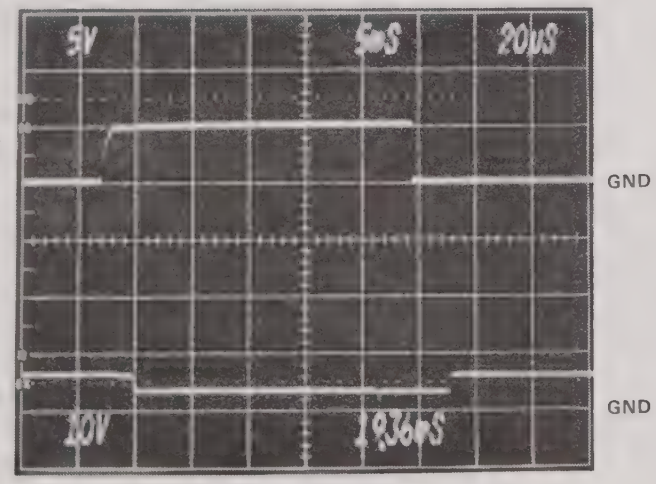
DATA I/O


5V
5mS
50µS
VCCP
VCCN
VCC
GND
E2
GND
5V
1.12mS

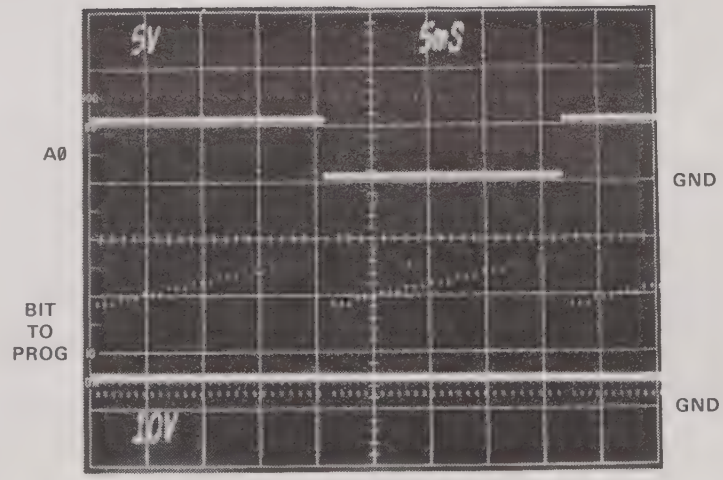
1


5V
5mS
20µS
E2
GND
TPW
TR
VOP
BIT
TO
PROG
GND
10V
1.36mS

2


5V
5mS
20µS
E2
GND
BIT
NO
PROG
GND
10V
1.36mS

3


5V
5mS
A0
GND
BIT
TO
PROG
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.3	5.5	5.7	V	
	VCCN	4.75	5.0	5.25	V	
	VOPB	17.5	18.0	18.5	V	See Note 3
	VOPE	25.5	26.0	26.5	V	See Note 3
	TPW	10.0		40.0	μ	See Note 4
	TR	42	52	70	μ	See Note 5
	Reject		27		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1998/TP4
	High Load	17.3	18.3	19.3	V	701-1998/TP2
	Low Load	17.3	18.3	19.3	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1998/TP4
	High Load	0.0	0.0	0.4	V	701-1998/TP2
	Low Load	4.7	5.7	6.7	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family E7.*
2. *Load RAM with hex 01 for Family E8.*
3. *These levels incrememt in 1-volt steps.*
4. *This is measured at the 90% level, and all nine levels must meet this spec.*
5. *This is measured from 10% to 90% on the tallest pulse.*

REVISIONS

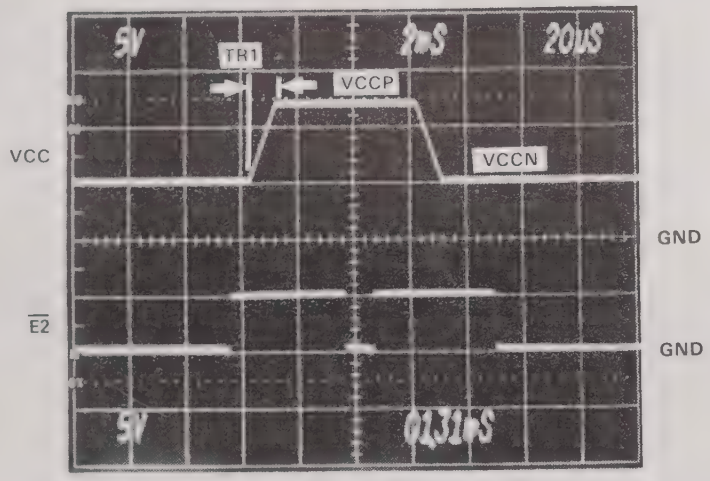
LTR	DESCRIPTION	P.E.	DATE

Sheet 1 of 1

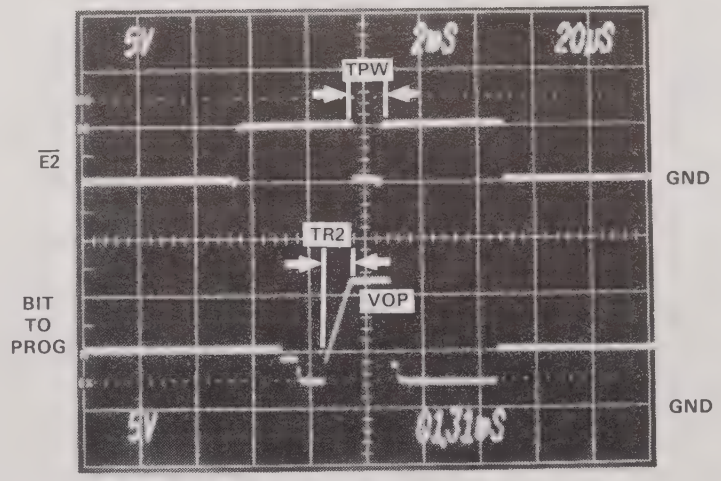
TIMING DIAGRAM

FAMILY CODES E7, E8

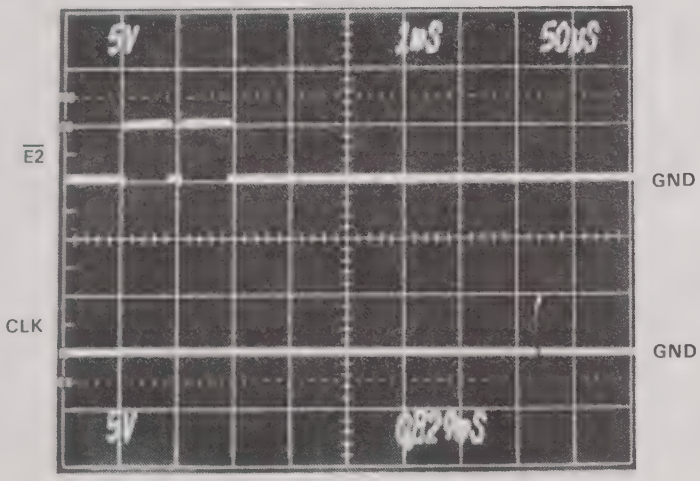
DATA I/O


5V
2mS
20µS
TR1
VCCP
VCCN
VCC
GND
E2
GND
5V
0.131mS

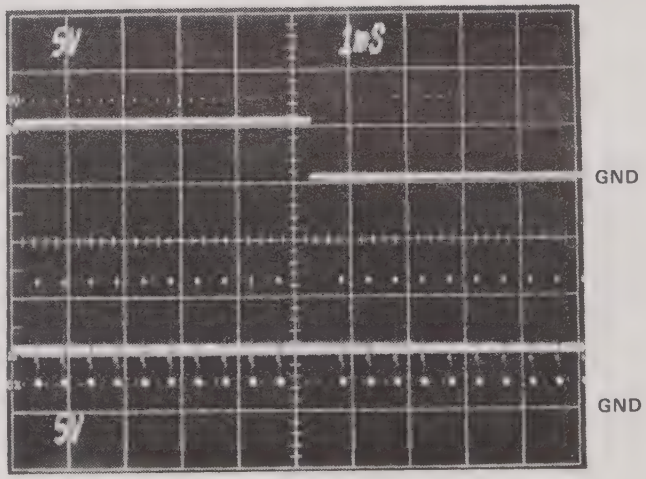
1


5V
2mS
20µS
TPW
E2
GND
TR2
VOP
BIT
TO
PROG
GND
5V
0.131mS

2


5V
1mS
50µS
E2
GND
CLK
GND
5V

3


5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.5	11.7	11.9	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	10.5	11.0	11.5	V	
	TPW	9.0	10.0	11.0	μs	
	TR1	10.0		20.0	μs	See Note 3
	TR2	5.0		18.0	μs	
	Reject		10		Pulses	
	Overprogram		5		Pulses	
1ST PASS VERIFY	VCC	4.2	4.3	4.4	V	
	VREF	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	6.4	7.4	8.4	V	701-1998/TP2
	LOW LOAD	6.4	7.4	8.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1998/TP4
	High Load	7.2	8.2	9.2	V	701-1998/TP2
	Low Load	7.2	8.2	9.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family EB.*
2. *Load RAM with hex 01 for Family EC.*
3. *Load VCC with a 100Ω, 2-watt resistor.*

REVISIONS

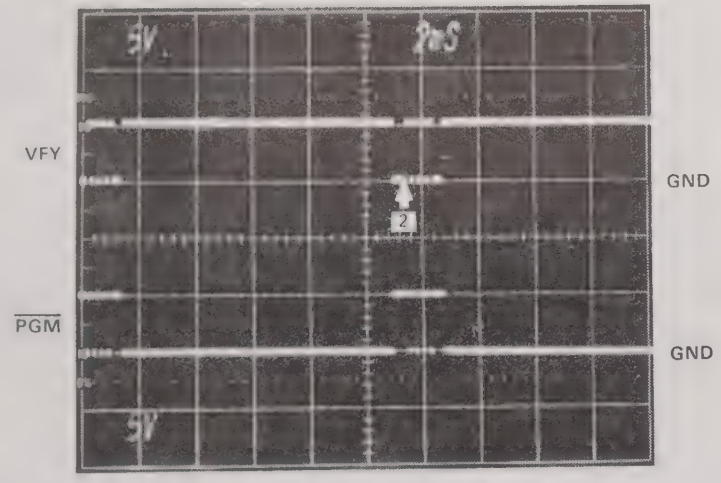
LTR	DESCRIPTION	P.E.	DATE

Sheet 1 of 1

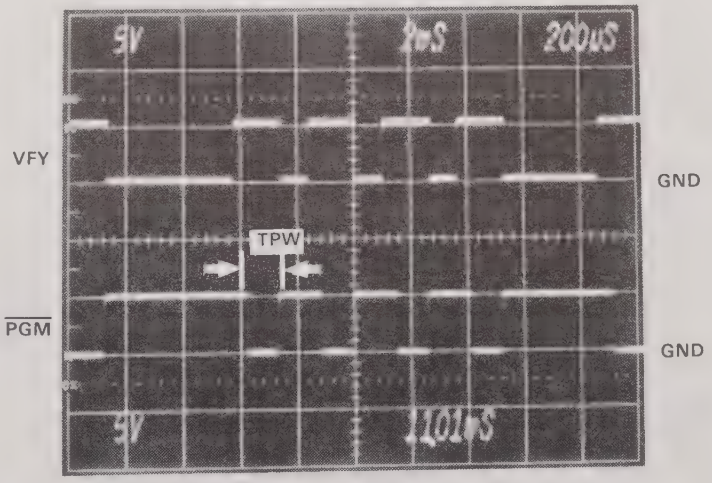
TIMING DIAGRAM

FAMILY CODES EB, EC

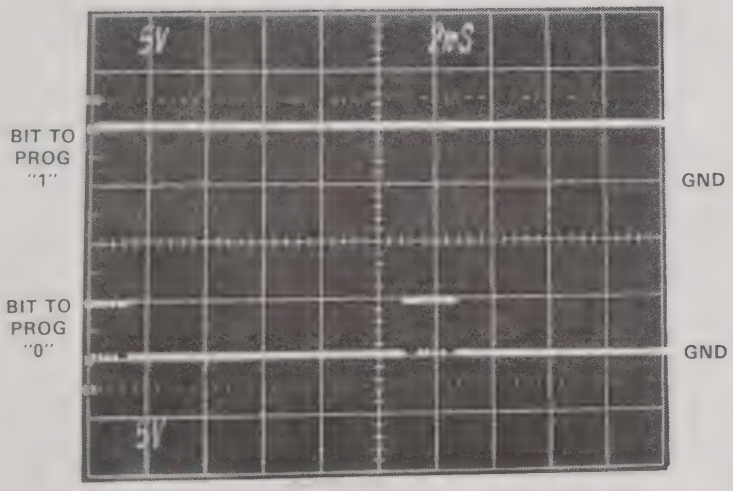
DATA I/O


5V
2mS
VFY
GND
2
PGM
GND
5V

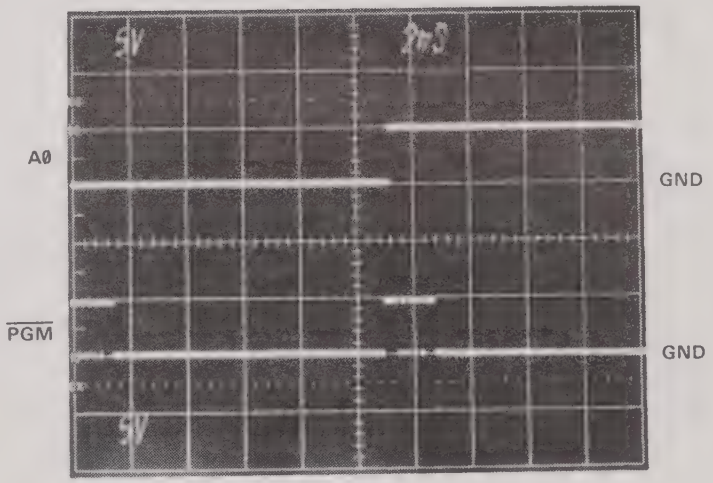
1


5V
2mS
200μS
VFY
GND
TPW
PGM
GND
5V
100μS

2


5V
2mS
BIT TO
PROG
"1"
GND
BIT TO
PROG
"0"
GND
5V

3


5V
2mS
A0
GND
PGM
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VPP	13.0	13.5	14.0	V	Not Shown
	TPW	95	100	105	μs	
	Reject		4		Pulses	
	Overprogram		1		Pulse	See Note 3
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	3.9	4.9	5.9	V	701-1998/TP3

NOTES

1. *Load RAM with hex 01 for both families.*
2. *Both zeros and ones have to be programmed.*
3. *The overprogram pulse is 2.4 ms times the number of programming pulses required to program the location.*

REVISIONS

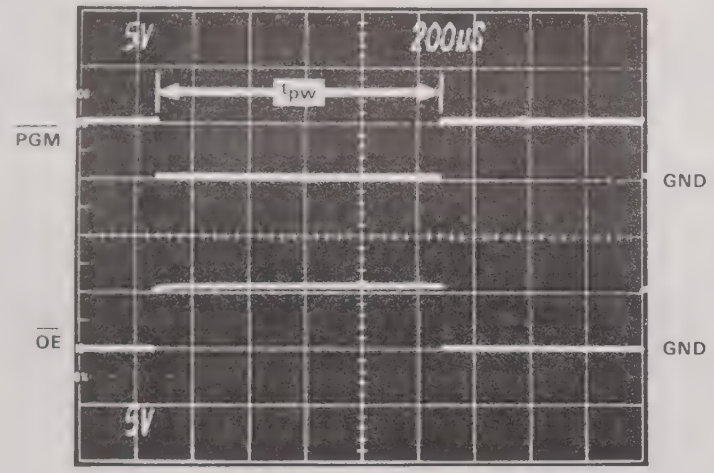
LTR	DESCRIPTION	P.E.	DATE

Sheet 1 of 1

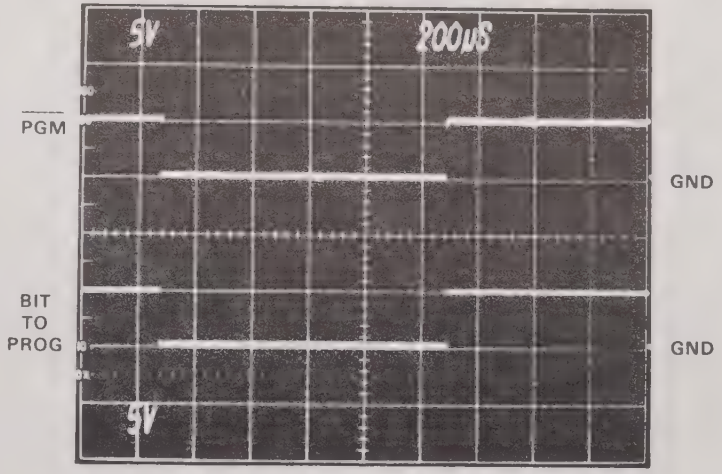
TIMING DIAGRAM

FAMILY CODES ED, EE

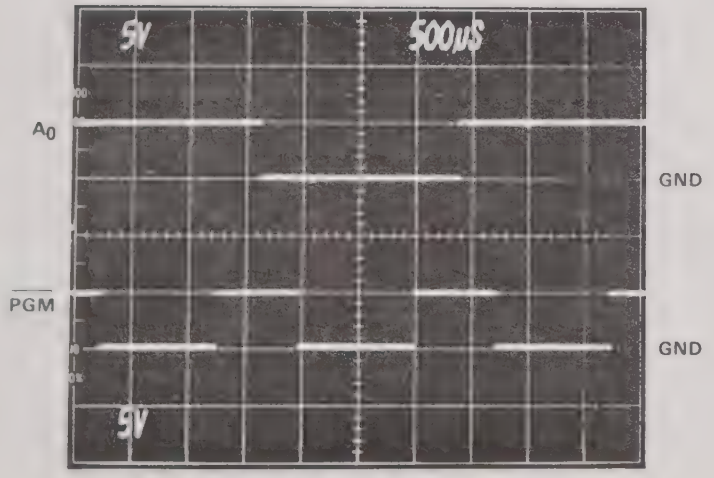
DATA I/O


5V
200uS
tpw
PGM
GND
OE
GND
5V

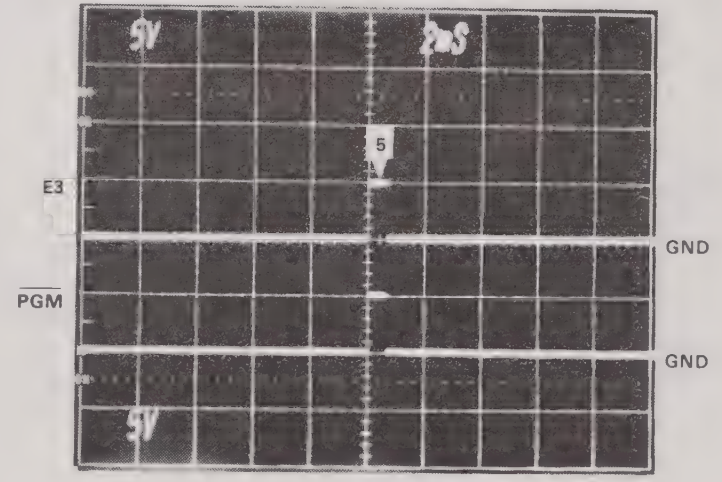
1


5V
200uS
PGM
GND
BIT
TO
PROG
GND
5V

2


5V
500uS
A0
GND
PGM
GND
5V

3


5V
2mS
5
E3
GND
PGM
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_{ew}	9.5	10.0	10.5	ms	
	t_f					N.A.
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.4	22.4	23.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	7.4	7.9	8.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family B9.*
2. *Photos 4-7 are chip-erase photos.*

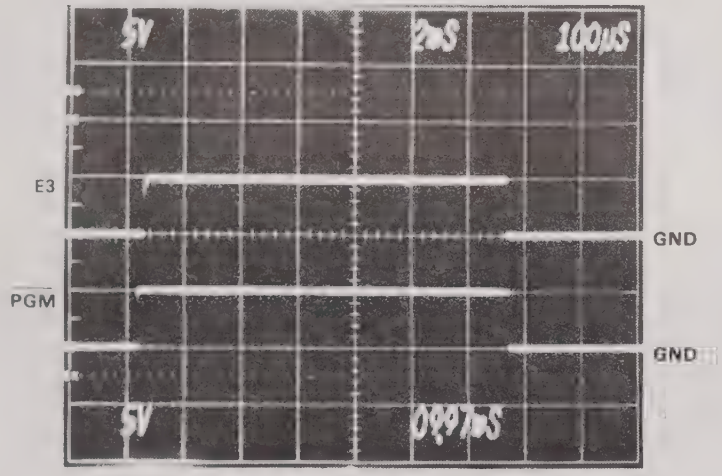
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

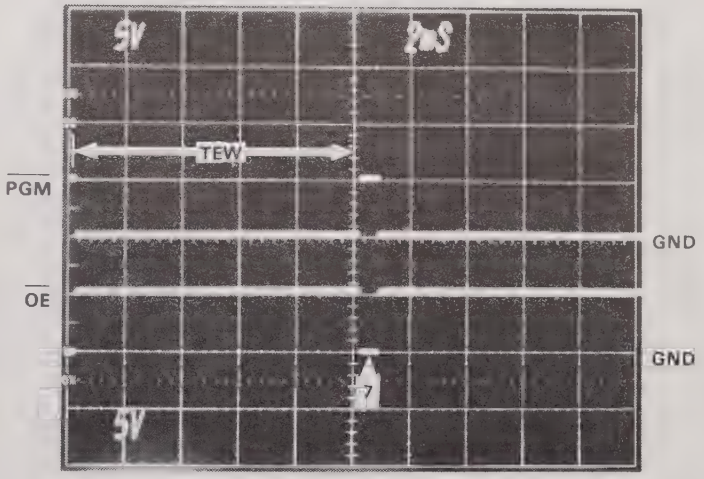
TIMING DIAGRAM

FAMILY CODES F1, F2

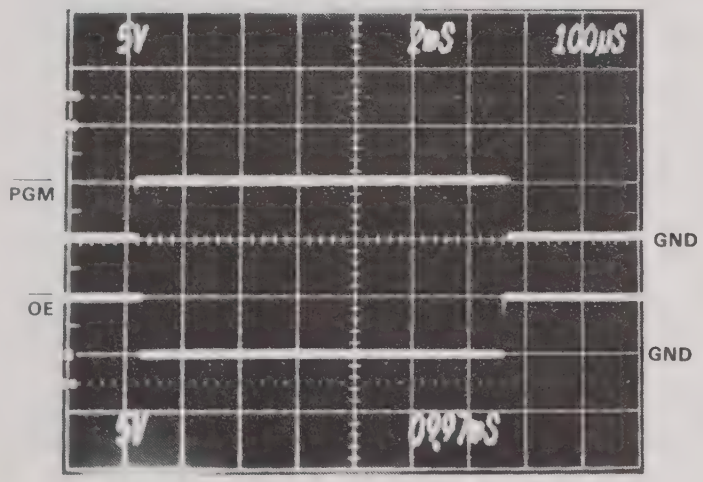
DATA I/O


5V
2mS
100µS
E3
GND
PGM
GND
5V

5


5V
2mS
TEW
PGM
GND
OE
GND
5V

6


5V
2mS
100µS
PGM
GND
OE
GND
5V

7

B-251
981-0003

REVISIONS

LTR	DESCRIPTION	P.E.	DATE

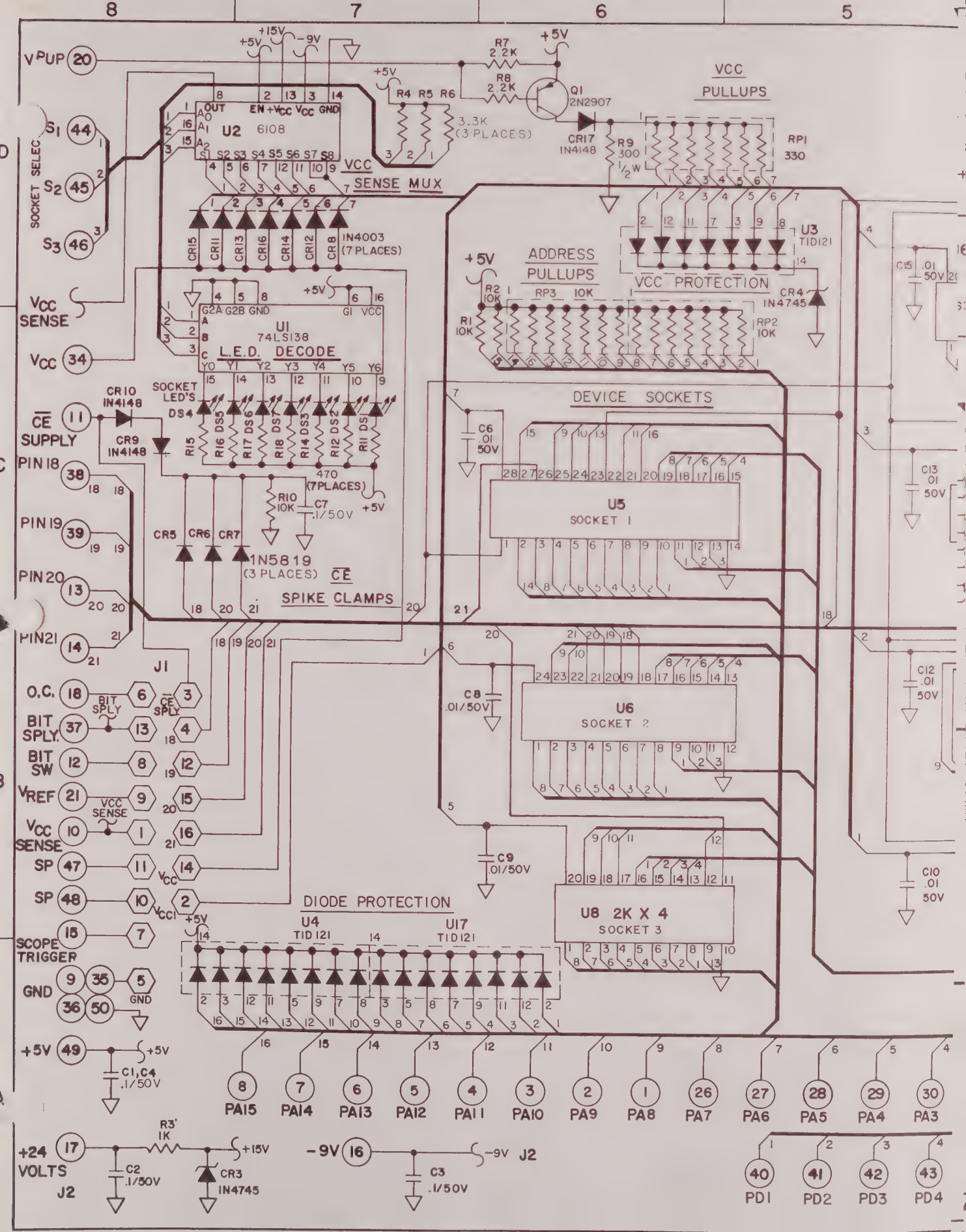
TIMING DIAGRAM

FAMILY CODES F1, F2

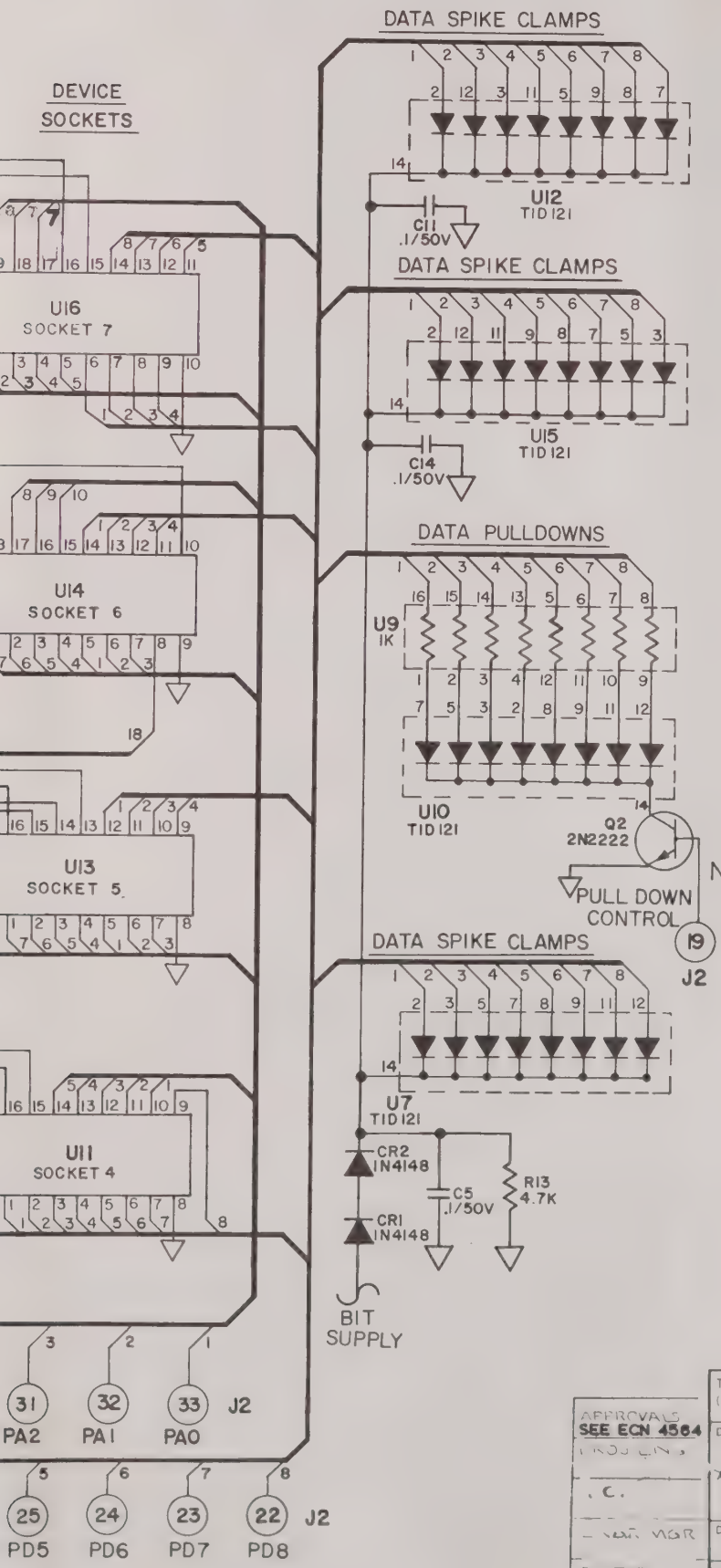
DATA I/O

APPENDIX C
SCHEMATICS

008-1998	Address Card
008-1999	Motherboard
30-701-7997	Waveform Generator
30-702-0045	UniPak™ Memory
30-702-7995	Socket Assembly


8
7
6
5
VPUP 20
+15V
+5V
-9V
R7 2.2K
R8 2.2K
+5V
Q1 2N2907
VCC PULLUPS
CR17 IN4148
R9 300 1/2 W
RP1 330
S1 44
S2 45
S3 46
SOCKET SELEC
U2 6108
OUT EN +Vcc Vcc GND
A0 A1 A2
S2 S3 S4 S5 S6 S7 S8
R4 R5 R6
3.3K (3 PLACES)
VCC SENSE MUX
CR15 CR11 CR13 CR16 CR14 CR12 CR8
IN4003 (7 PLACES)
U3 TID121
VCC PROTECTION
CR4 IN4745
+5V
ADDRESS PULLUPS
R2 10K
RP3 10K
R1 10K
RP2 10K
VCC SENSE
VCC 34
U1 74LS138
G2A G2B GND G1 VCC
L.E.D. DECODE
Y0 Y1 Y2 Y3 Y4 Y5 Y6
SOCKET LED'S
DS4
R15 R16 DS5 R17 DS6 R18 DS7 R14 DS3 R12 DS2 R11 DS1
470 (7PLACES)
CR10 IN4148
CR9 IN4148
CE SUPPLY 11
R10 10K
C7 .1/50V
DEVICE SOCKETS
C6 .01 50V
U5 SOCKET 1
PIN 18 38
PIN 19 39
PIN 20 13
PIN 21 14
CR5 CR6 CR7
1N5819 (3 PLACES) CE
SPIKE CLAMPS
J1
O.C. 18
BIT SPLY. 37
BIT SW 12
VREF 21
VCC SENSE 10
SP 47
SP 48
SCOPE TRIGGER 15
GND 9 35 36 50
C8 .01/50V
U6 SOCKET 2
C9 .01/50V
U8 2K X 4 SOCKET 3
C10 .01 50V
C12 .01 50V
C13 01 50V
C15 .01 50V
DIODE PROTECTION
U4 TID121
U17 TID121
+5V 49
C1, C4 .1/50V
PA15 8
PA14 7
PA13 6
PA12 5
PA11 4
PA10 3
PA9 2
PA8 1
PA7 26
PA6 27
PA5 28
PA4 29
PA3 30
+24 VOLTS 17
R3' 1K
C2 .1/50V
CR3 IN4745
-9V 16
C3 .1/50V
J2
PD1 40
PD2 41
PD3 42
PD4 43

REVISIONS					
ZONE	LTR	DESCRIPTION			
	A	RELEASE PER ECN 4564			5/82
	B	ECN 4728			1/83



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4 W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED:

U17	CR17
RP3	C15
R18	J2
DS7	Q2

APPROVALS SEE ECN 4564

TOLERANCES (EXCEPT AS NOTED)

DECIMAL ±

ANGULAR ±

DRAWN BY G. RYDER

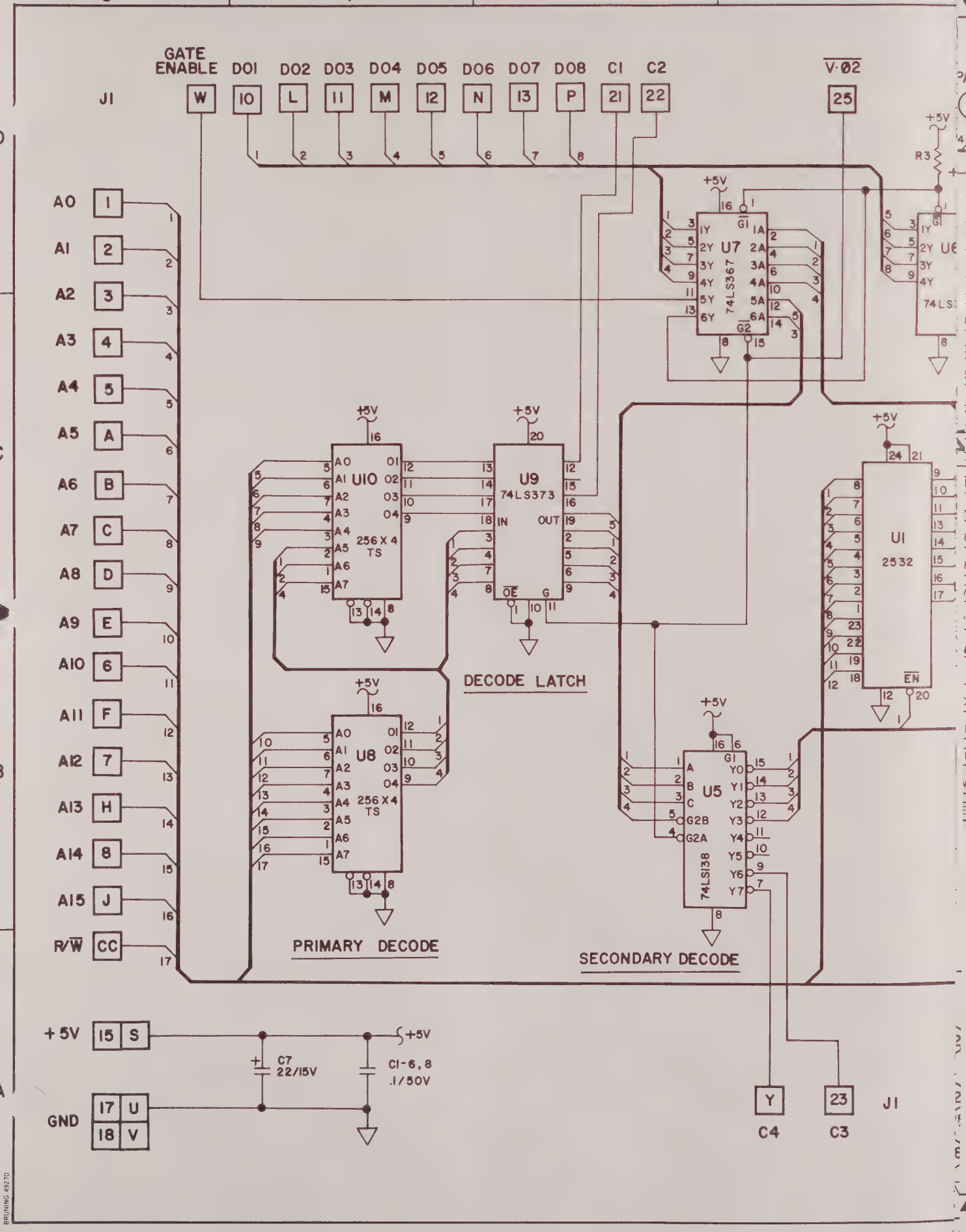
CHECKED BY:

DATA I/O

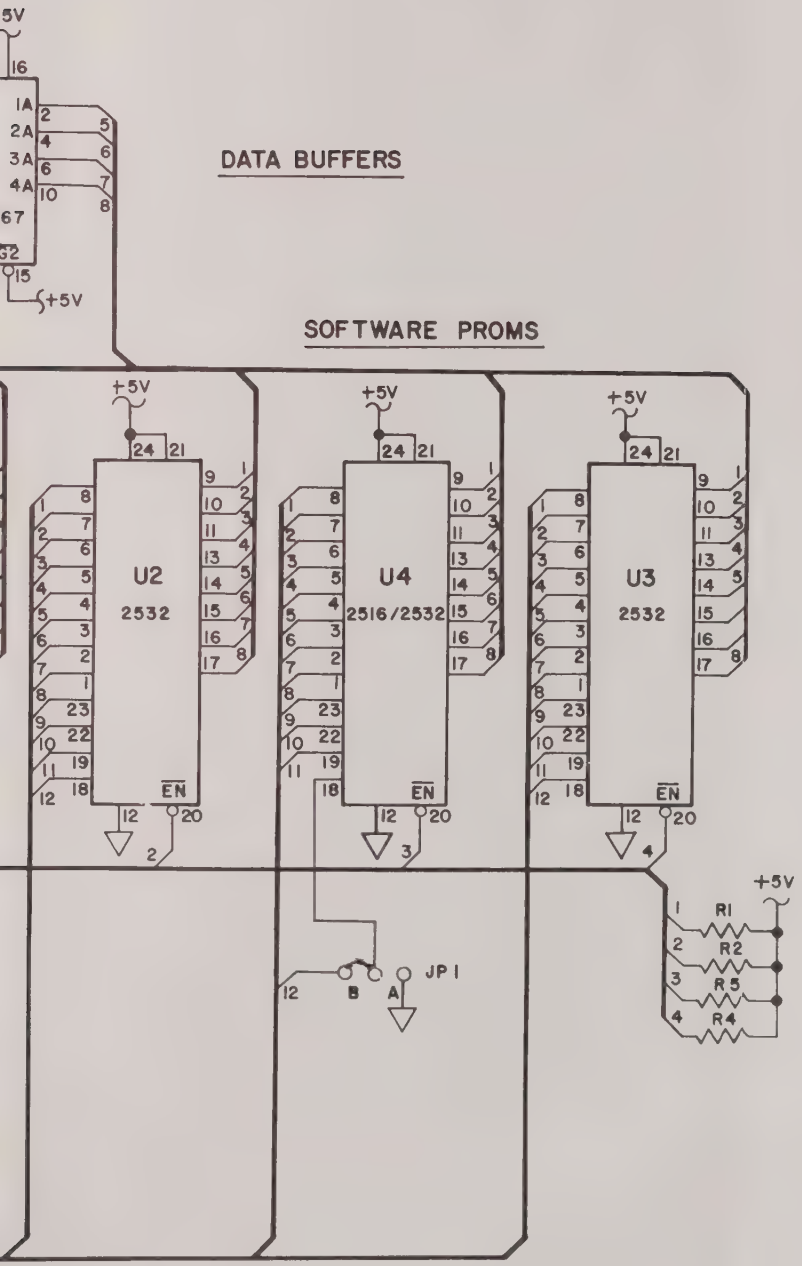
TITLE SCHEMATIC DIAGRAM UniPak SOCKET ASSEMBLY

SIZE D | CODE IDENT NO | DRAWING NO 30-702-7995

SHEET 1 OF 1


GATE ENABLE
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
C1
C2
V·Ø2
J1
W
10
L
11
M
12
N
13
P
21
22
25
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
R/W
1
2
3
4
5
A
B
C
D
E
6
F
7
H
8
J
CC
U7
74LS367
U10
256 X 4
TS
U9
74LS373
U8
U1
2532
U5
74LS138
R3
+5V
DECODE LATCH
PRIMARY DECODE
SECONDARY DECODE
+5V
15
S
GND
17
U
18
V
C7
22/15V
C1-6, 8
.1/50V
Y
C4
23
C3
J1

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	TC	[illegible]	[illegible]	5·4·81
B	INCORPORATED ECP 0061 ADCN A1		[illegible]	[illegible]	

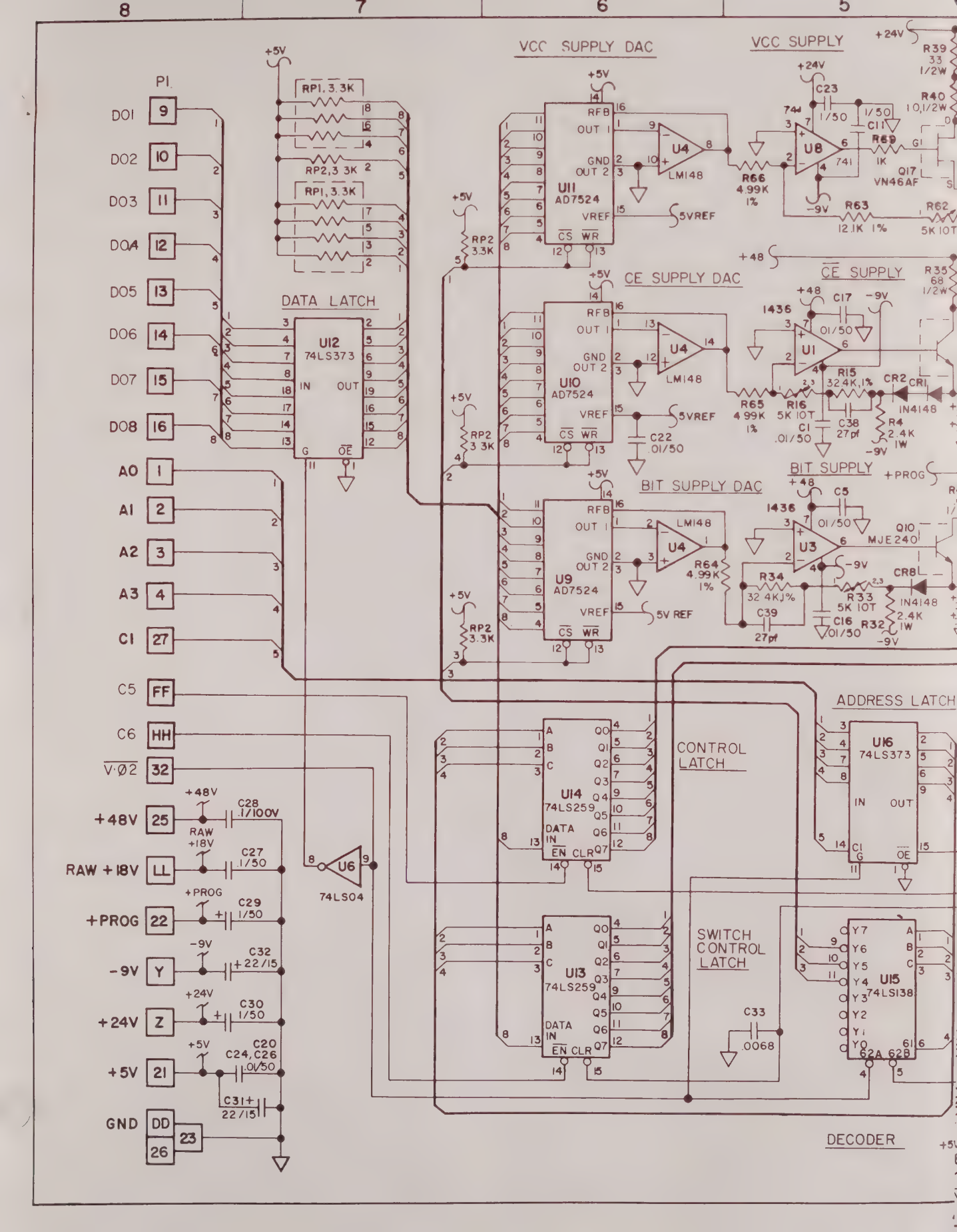


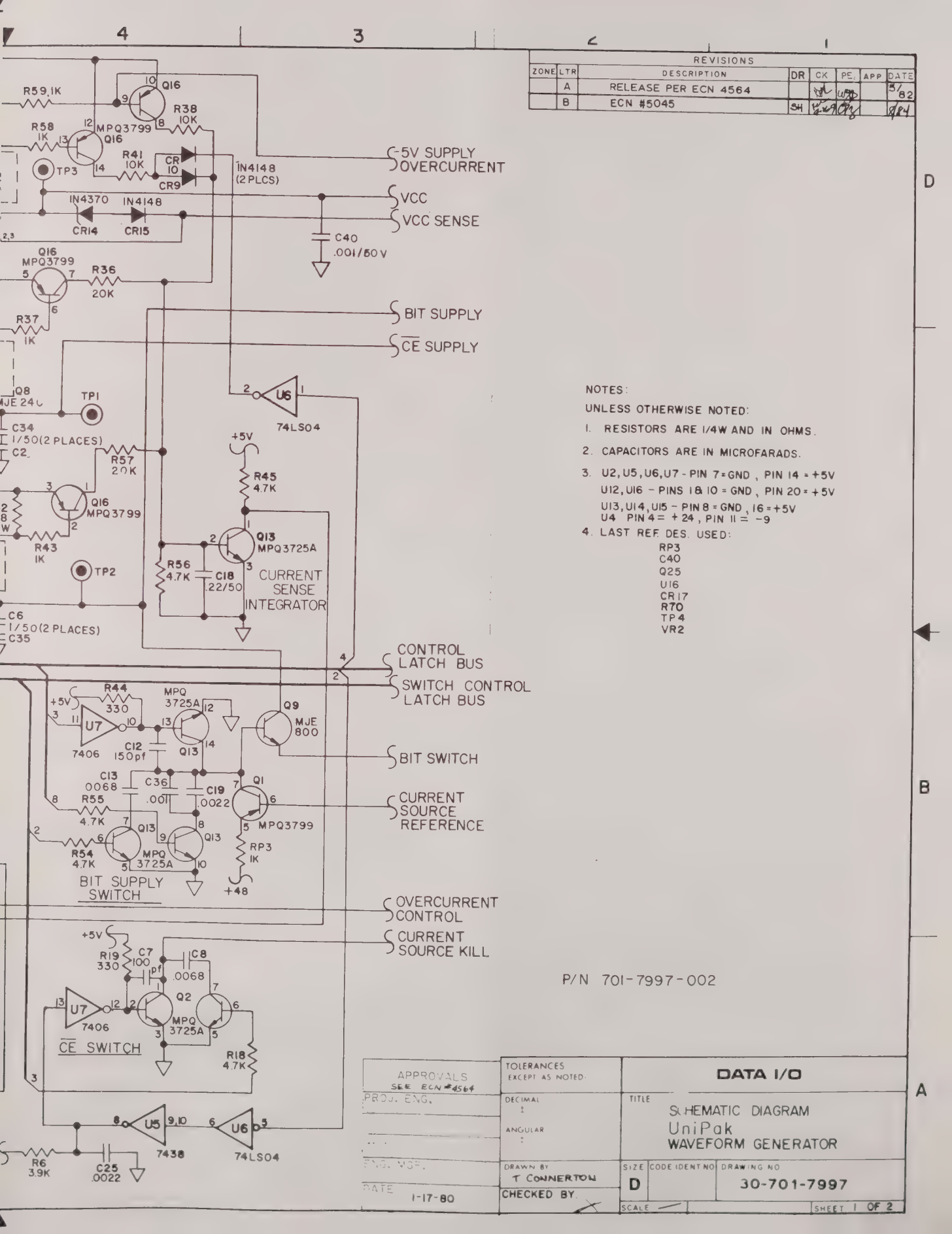
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 3.3K OHMS 1/4W 5%
2. ALL CAPACITORS ARE IN MICROFARADS.
3. JP 1, POS. A
4. LAST REFERENCE DESIGNATOR USED:
   C8
   R5
   U10
   JP 1

P/N 702-0045-002

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O ISSAQUAH, WASH		
DSN. ENGR [signature]	DATE 5/5/81	TOLERANCES, UNLESS OTHERWISE SPECIFIED: XX ± XXX ± ANGULAR		TITLE SCHEMATIC DIAGRAM UNIPAK MEMORY		
MFG ENGR [signature]	DATE [illegible]					
QUAL ASSUR. [signature]	DATE 5-6-81	DRAWN BY: TCC	DATE 3-16-81	SIZE D	CODE INDENT NO 54193	DRAWING NO 30-702-0045
ENGR. MGR. [signature]	DATE 5-5-81	CHECKED BY: [signature]	DATE 5-4-81	SCALE NONE		SHEET 1 OF 1


8
7
6
5
P1
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
A0
A1
A2
A3
C1
C5
C6
V·Ø2
+48V
RAW +18V
+PROG
-9V
+24V
+5V
GND
RP1, 3.3K
RP2, 3.3K
RP1, 3.3K
DATA LATCH
U12
74LS373
IN
OUT
G
OE
VCC SUPPLY DAC
U11
AD7524
RFB
OUT 1
OUT 2
GND
VREF
CS
WR
U4
LM148
5VREF
R66
4.99K
1%
VCC SUPPLY
U8
741
R39
33
1/2W
R40
10,1/2W
R69
1K
Q17
VN46AF
R63
12.1K 1%
R62
5K 10T
CE SUPPLY DAC
U10
AD7524
C22
.01/50
CE SUPPLY
U1
R35
68
1/2W
R15
32.4K,1%
R16
5K 10T
R65
4.99K
1%
C1
.01/50
C38
27pf
R4
2.4K
1W
CR2
CR1
IN4148
BIT SUPPLY DAC
U9
AD7524
5V REF
BIT SUPPLY
U3
Q10
MJE240
R64
4.99K
1%
R34
32.4KJ%
C39
27pf
R33
5K 10T
C16
.01/50
R32
2.4K
1W
CR8
IN4148
RP2
3.3K
C28
.1/100V
C27
.1/50
C29
1/50
C32
22/15
C30
1/50
C20
C24, C26
.01/50
C31
22/15
U6
74LS04
CONTROL LATCH
U14
74LS259
DATA IN
EN
CLR
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
ADDRESS LATCH
U16
74LS373
SWITCH CONTROL LATCH
U13
74LS259
C33
.0068
U15
74LS138
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
62A
62B
DECODER



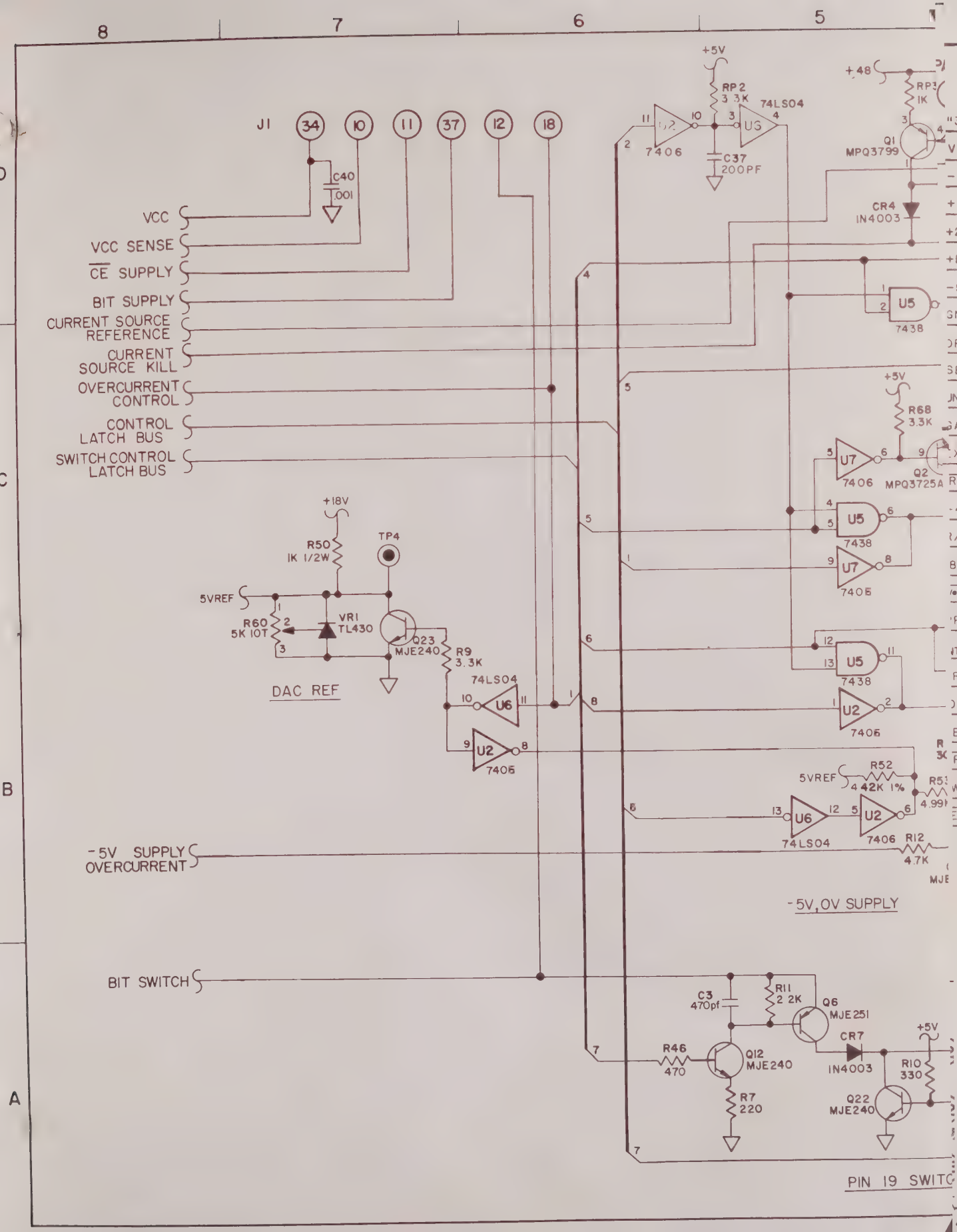
NOTES:

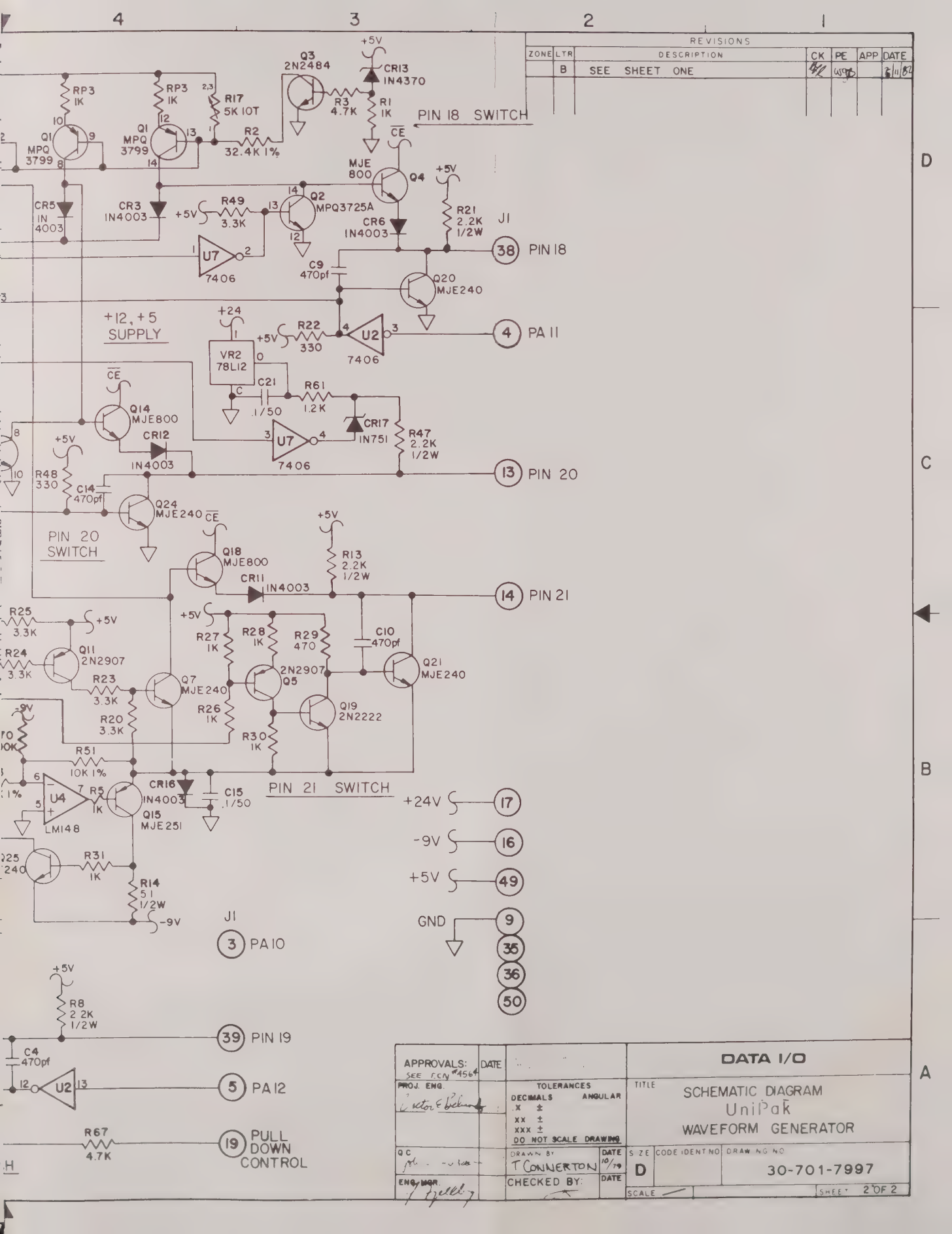
UNLESS OTHERWISE NOTED:

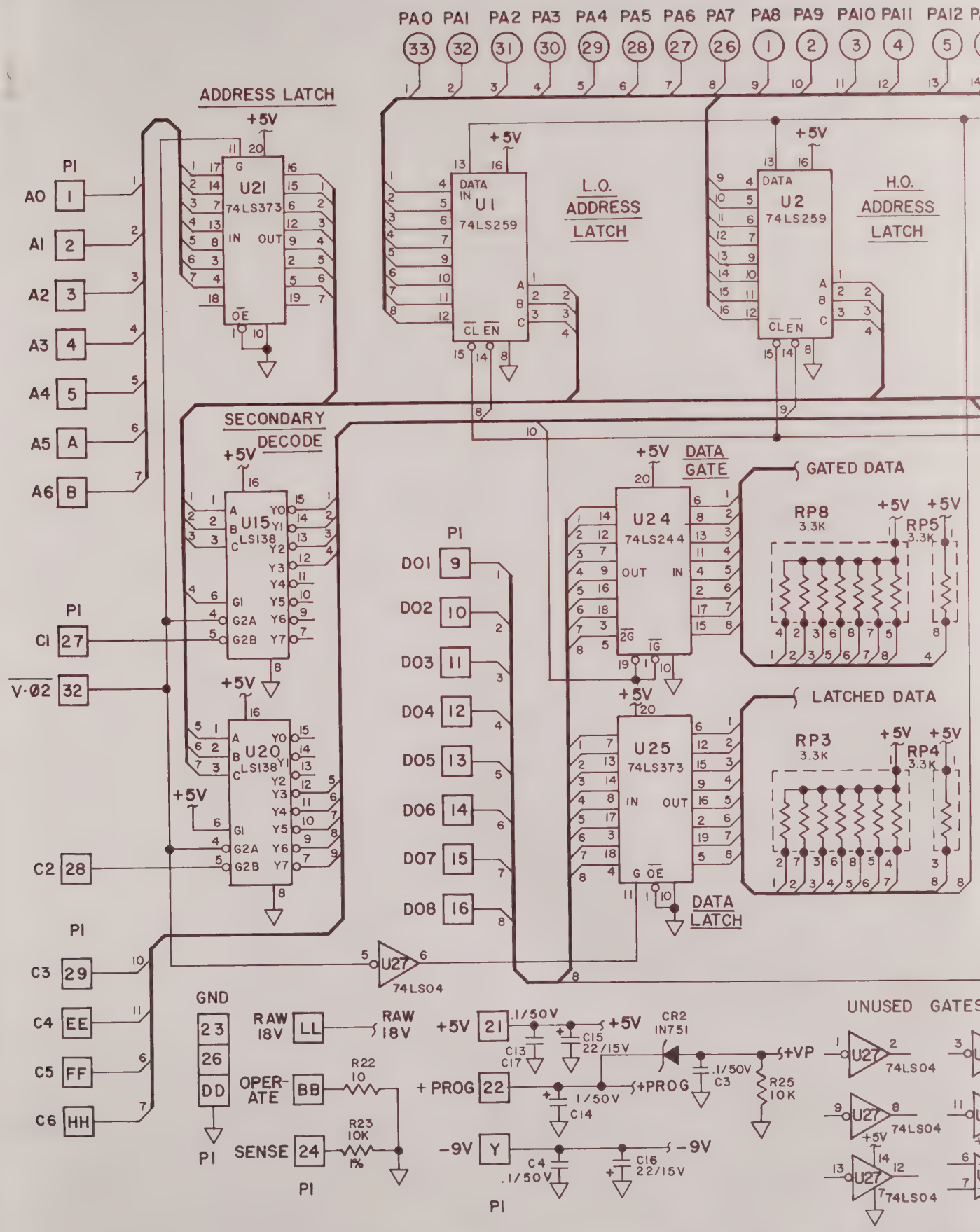
1. RESISTORS ARE 1/4W AND IN OHMS.
2. CAPACITORS ARE IN MICROFARADS.
3. U2, U5, U6, U7 - PIN 7 = GND, PIN 14 = +5V
   U12, U16 - PINS 18 10 = GND, PIN 20 = +5V
   U13, U14, U15 - PIN 8 = GND, 16 = +5V
   U4 PIN 4 = +24, PIN 11 = -9
4. LAST REF DES. USED:
   RP3
   C40
   Q25
   U16
   CR17
   R70
   TP4
   VR2

P/N 701-7997-002

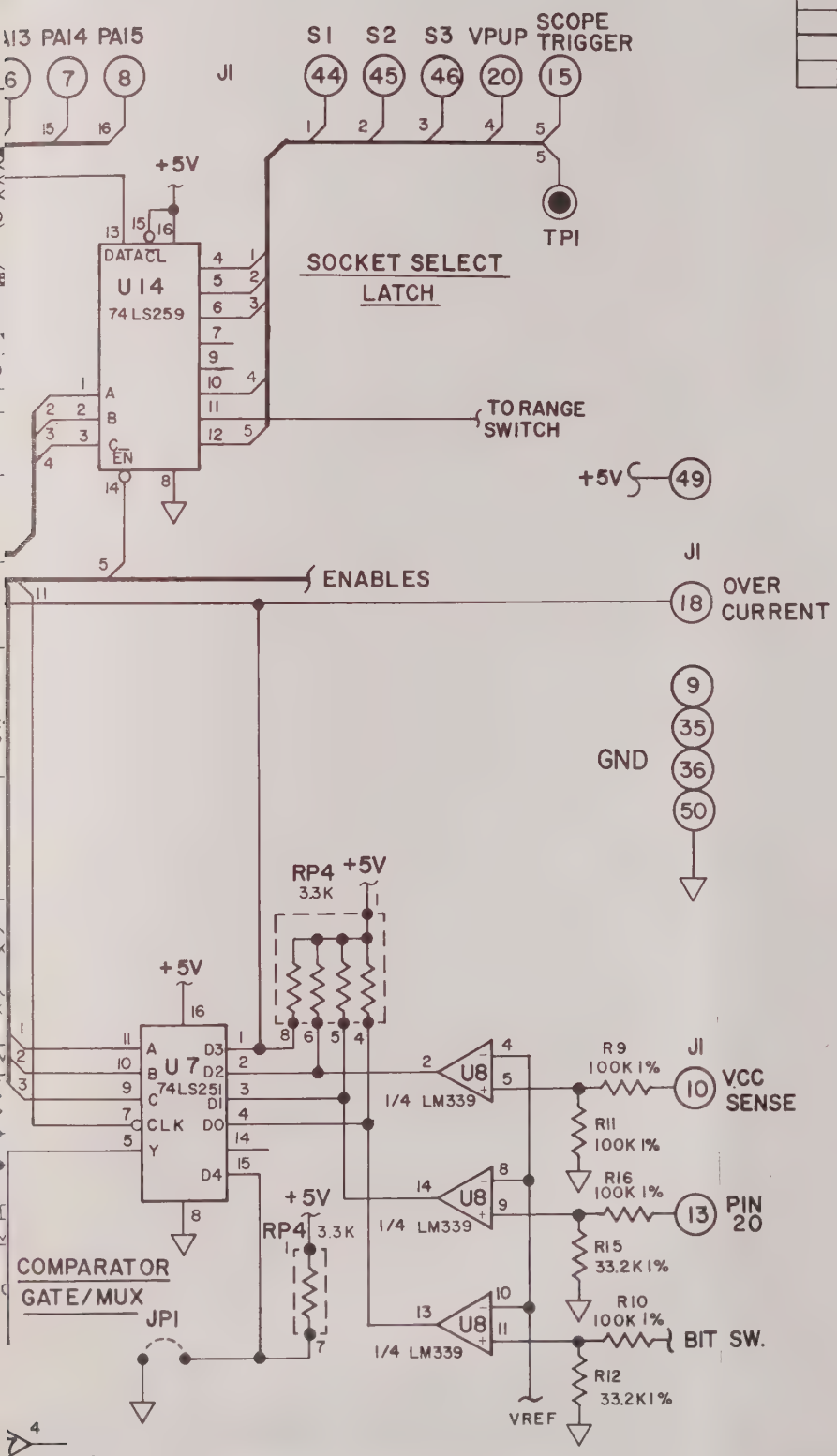
APPROVALS	TOLERANCES EXCEPT AS NOTED:	DATA I/O
SEE ECN #4564	DECIMAL ±	TITLE: SCHEMATIC DIAGRAM UniPak WAVEFORM GENERATOR
PROJ. ENG.	ANGULAR ±	
PROD. MGR.	DRAWN BY: T. CONNERTON	SIZE: D; CODE IDENT NO: ; DRAWING NO: 30-701-7997
DATE: 1-17-80	CHECKED BY:	SCALE: ; SHEET 1 OF 2


8
7
6
5
J1
34
10
11
37
12
18
C40
.001
VCC
VCC SENSE
CE SUPPLY
BIT SUPPLY
CURRENT SOURCE REFERENCE
CURRENT SOURCE KILL
OVERCURRENT CONTROL
CONTROL LATCH BUS
SWITCH CONTROL LATCH BUS
+5V
RP2
3.3K
74LS04
U3
U2
7406
C37
200PF
+48
RP3
1K
Q1
MPQ3799
CR4
IN4003
U5
7438
R68
3.3K
U7
7406
Q2
MPQ3725A
+18V
R50
1K 1/2W
TP4
5VREF
R60
5K 10T
VR1
TL430
Q23
MJE240
R9
3.3K
DAC REF
U6
74LS04
R52
4.42K 1%
R51
4.99K
R12
4.7K
-5V SUPPLY OVERCURRENT
-5V,0V SUPPLY
BIT SWITCH
C3
470pf
R11
2.2K
Q6
MJE251
CR7
IN4003
R46
470
Q12
MJE240
R7
220
R10
330
Q22
MJE240
PIN 19 SWITC


4
3
2
1
REVISIONS
ZONE LTR DESCRIPTION CK PE APP DATE
B SEE SHEET ONE 3/11/82
PIN 18 SWITCH
Q3 2N2484
CR13 IN4370
RP3 1K
RP3 1K
RI7 5K 10T
R3 4.7K
R1 1K
Q1 MPQ 3799
R2 32.4K 1%
MJE 800 Q4
CR5 IN 4003
CR3 IN4003
R49 3.3K
Q2 MPQ3725A
CR6 IN4003
R21 2.2K 1/2W
J1
38 PIN 18
U7 7406
C9 470pf
Q20 MJE240
+12, +5 SUPPLY
VR2 78L12
R22 330
U2 7406
4 PA 11
C21 .1/50
R61 1.2K
Q14 MJE800
CR12 IN4003
CR17 IN751
R47 2.2K 1/2W
13 PIN 20
R48 330
C14 470pf
Q24 MJE240
PIN 20 SWITCH
Q18 MJE800
CR11 IN4003
R13 2.2K 1/2W
14 PIN 21
R25 3.3K
Q11 2N2907
R24 3.3K
R23 3.3K
Q7 MJE240
R20 3.3K
R27 1K
R28 1K
R29 470
2N2907 Q5
C10 470pf
Q21 MJE240
R26 1K
Q19 2N2222
R30 1K
R51 10K 1%
U4 LM148
R5 1K
CR16 IN4003
Q15 MJE251
C15 .1/50
PIN 21 SWITCH
R31 1K
R14 51 1/2W
+24V 17
-9V 16
+5V 49
GND 9 35 36 50
J1
3 PA 10
R8 2.2K 1/2W
39 PIN 19
C4 470pf
U2
5 PA 12
R67 4.7K
19 PULL DOWN CONTROL
APPROVALS: SEE ECN #456
DATE
PROJ. ENG.
QC
ENG. MGR.
TOLERANCES
DECIMALS ANGULAR
.X ±
XX ±
XXX ±
DO NOT SCALE DRAWING
DRAWN BY T CONNERTON
DATE 10/79
CHECKED BY:
DATE
DATA I/O
TITLE
SCHEMATIC DIAGRAM
UniPak
WAVEFORM GENERATOR
SIZE D
CODE IDENT NO
DRAWING NO 30-701-7997
SCALE
SHEET 2 OF 2


PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11 PA12
33 32 31 30 29 28 27 26 1 2 3 4 5
ADDRESS LATCH
+5V
U21
74LS373
IN OUT
OE
PI
A0 1
A1 2
A2 3
A3 4
A4 5
A5 A
A6 B
U1
74LS259
DATA IN
CL EN
L.O. ADDRESS LATCH
U2
74LS259
H.O. ADDRESS LATCH
SECONDARY DECODE
U15
LS138
U20
LS138
G1 G2A G2B
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
C1 27
V·Ø2 32
C2 28
C3 29
C4 EE
C5 FF
C6 HH
DO1 9
DO2 10
DO3 11
DO4 12
DO5 13
DO6 14
DO7 15
DO8 16
DATA GATE
U24
74LS244
OUT IN
GATED DATA
RP8 3.3K
RP5 3.3K
U25
74LS373
IN OUT
G OE
LATCHED DATA
RP3 3.3K
RP4 3.3K
DATA LATCH
U27
74LS04
GND
23 26 DD
RAW 18V LL
OPER-ATE BB
SENSE 24
R22 10
R23 10K 1%
+5V 21
+PROG 22
-9V Y
C13 C17 .1/50V
C15 22/15V
C14 1/50V
C4 .1/50V
C16 22/15V
CR2 IN751
C3 .1/50V
R25 10K
+VP
UNUSED GATES

REVISIONS							
ZONE	LTR	DESCRIPTION	DR	CHK	CM	PE	DATE
	A	RELEASE					1-17-80
	B	ECN 3742					7-80
	C	ECN 5045	SH				1/84
	D	INCORP ADCN C1 PER ECP00000				RSS	6-12-6



NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS IN MICROFARADS.
3. LAST REF. DES. USED:
   U27 R25 TP4
   CR5 C17 J1
   RP8 Q19 JP1

P/N 701-1998

APPROVALS		
PROJ. ENG.		
ENG. MGR.		
DATE	1-4-80	CHECKED BY

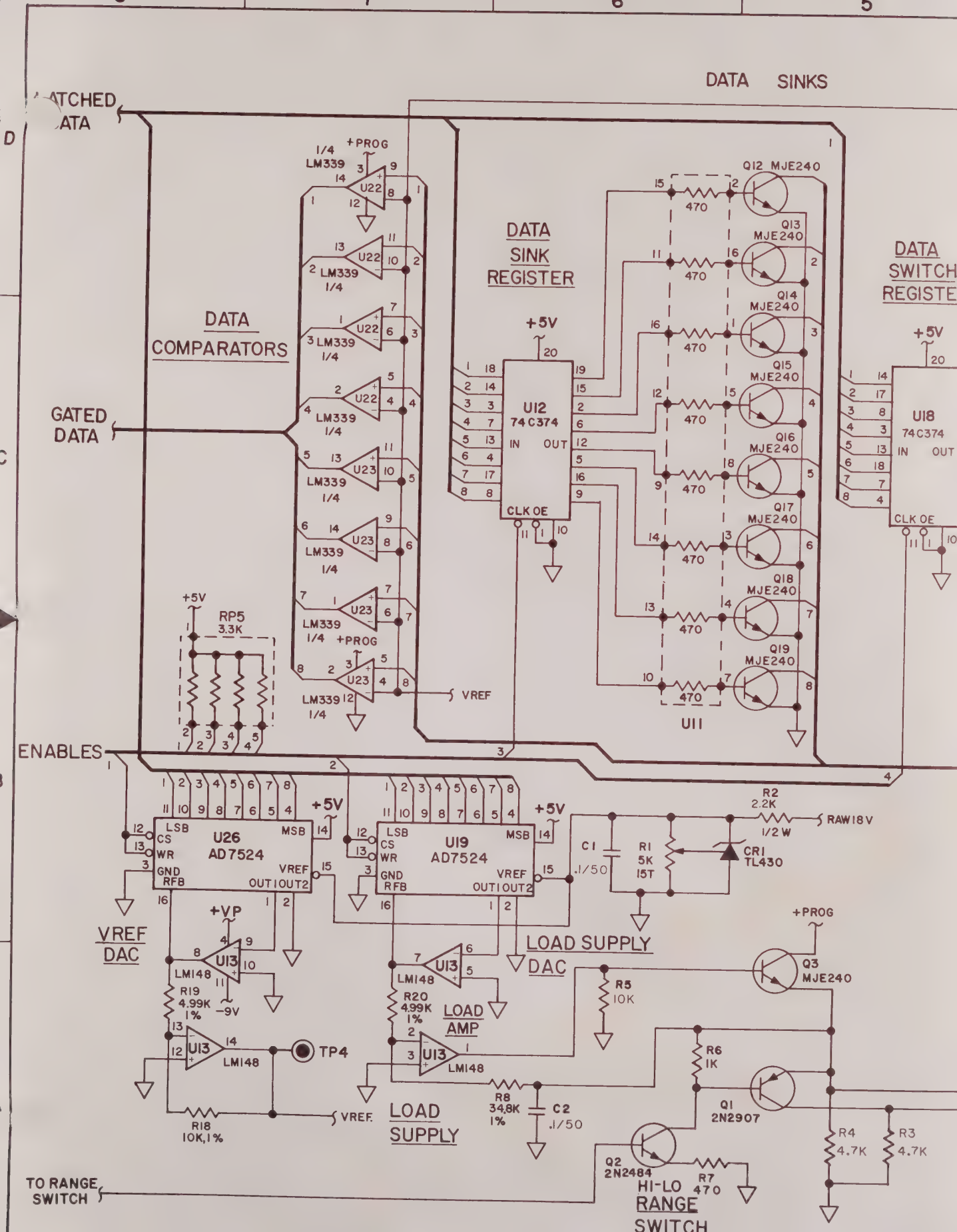
TOLERANCES (EXCEPT AS NOTED)
DECIMAL ±
ANGULAR ±
DRAWN BY:

DATA I/O ISSAQUAH WASH

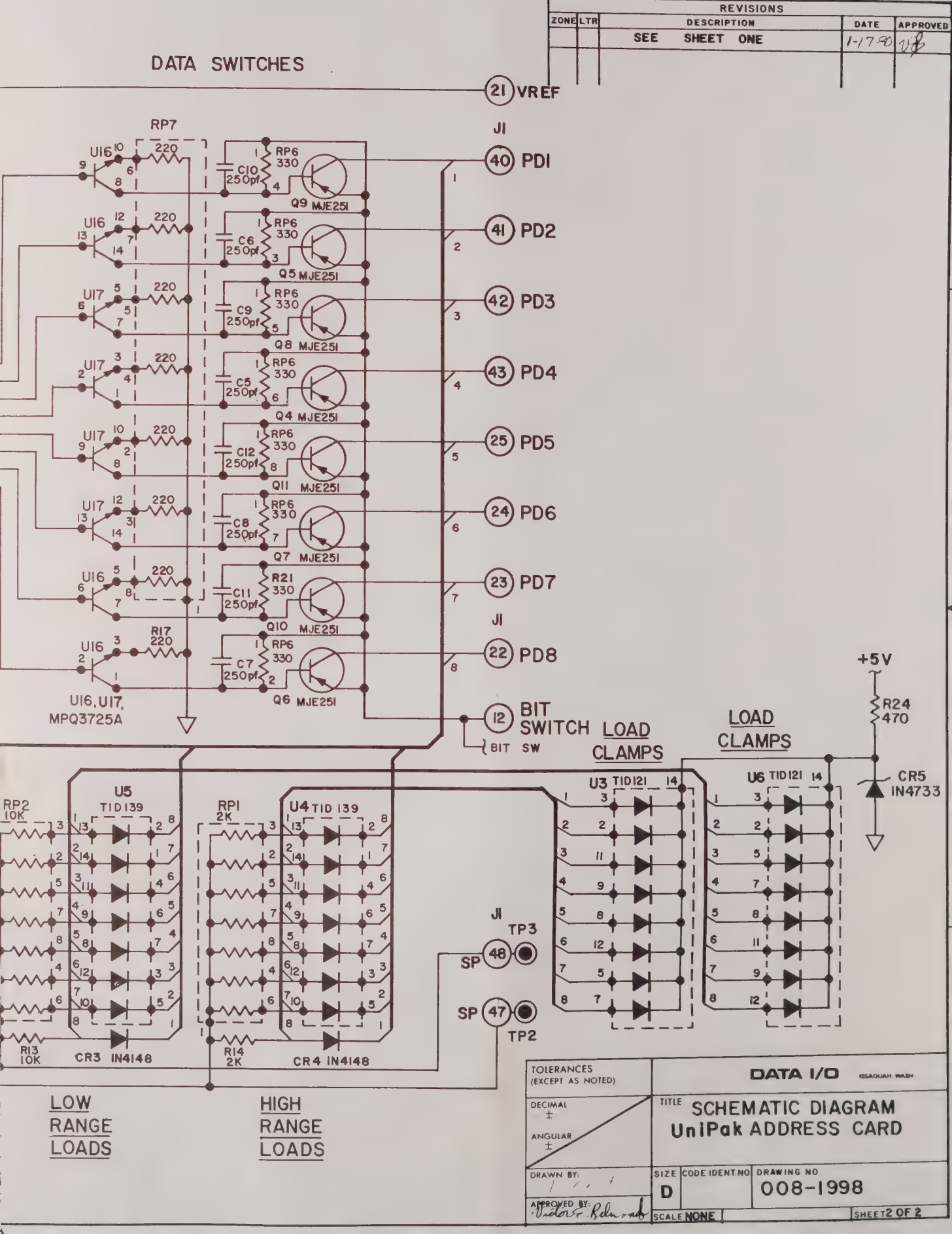
TITLE SCHEMATIC DIAGRAM
UniPak ADDRESS CARD

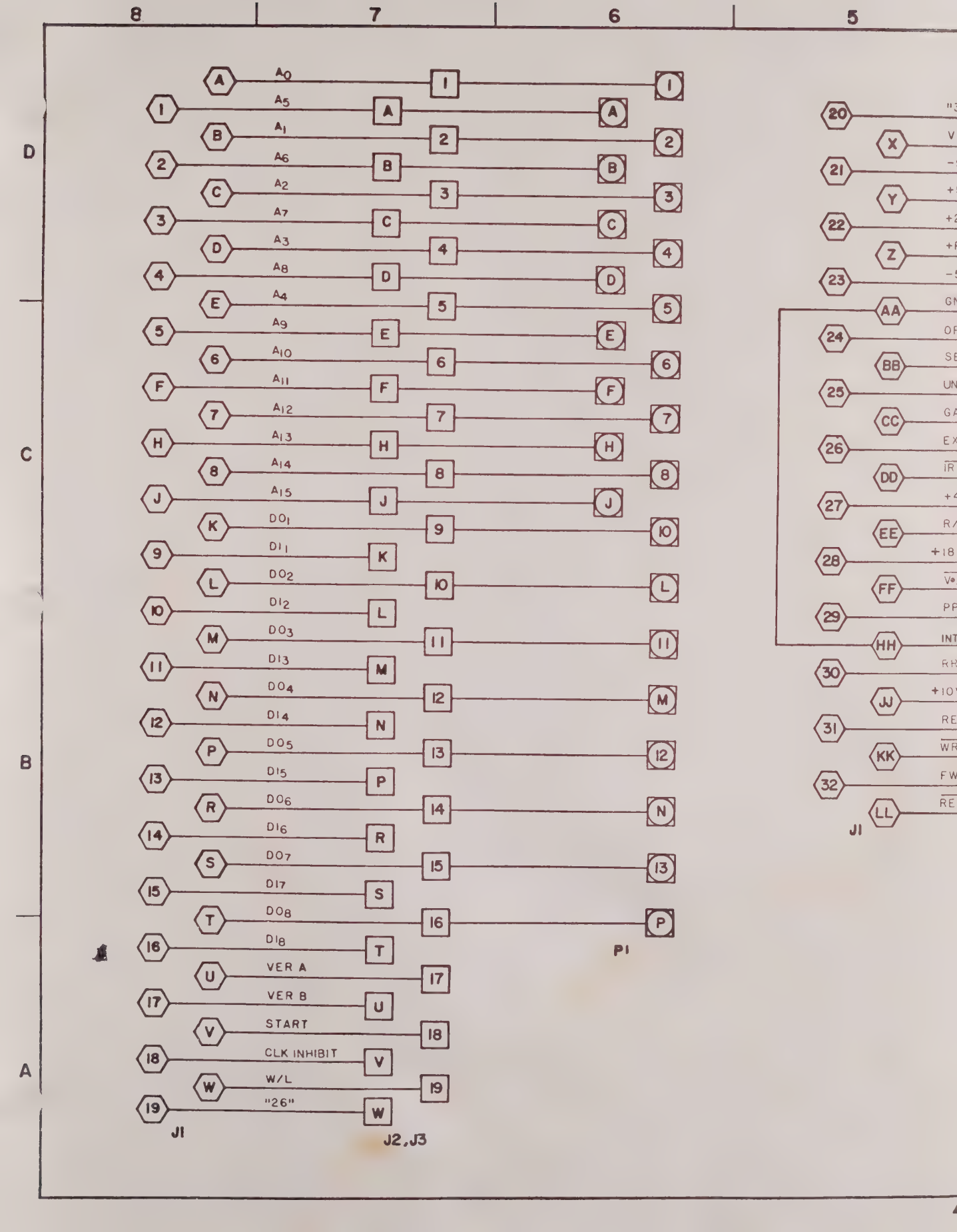
SIZE	CODE IDENT NO.	DRAWING NO
D		008-1998

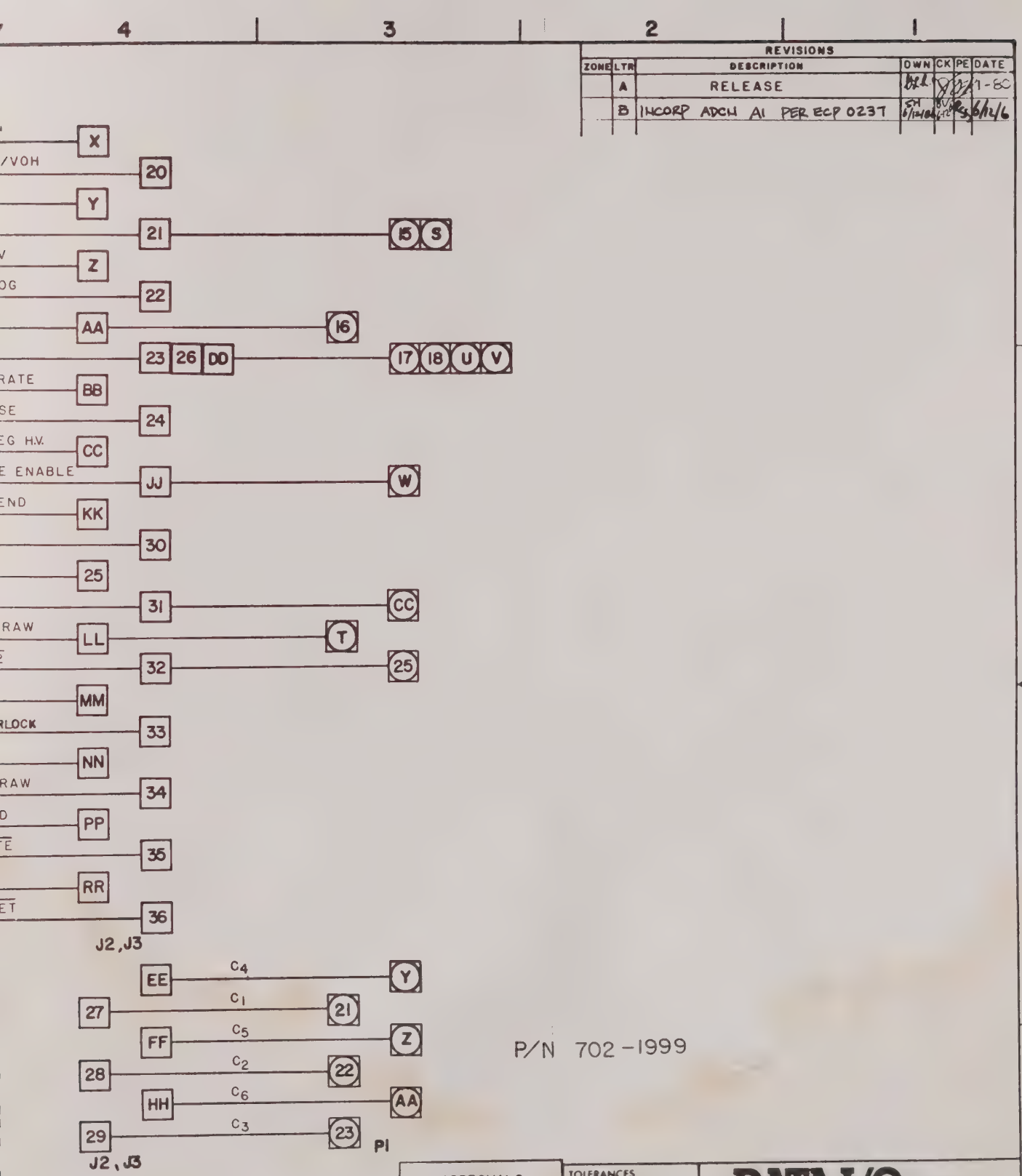
SCALE NONE SHEET 1 OF 2



DATA SINKS
ATCHED DATA
GATED DATA
ENABLES
DATA COMPARATORS
DATA SINK REGISTER
DATA SWITCH REGISTE
U12 74C374
U18 74C374
U11
U26 AD7524
U19 AD7524
VREF DAC
LOAD SUPPLY DAC
LOAD AMP
LOAD SUPPLY
HI-LO RANGE SWITCH
TO RANGE SWITCH
RAW18V
TP4
VREF
+PROG
+5V
+VP
-9V


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
SEE SHEET ONE 1-17-90
DATA SWITCHES
21 VREF
J1
40 PD1
41 PD2
42 PD3
43 PD4
25 PD5
24 PD6
23 PD7
J1
22 PD8
12 BIT SWITCH
BIT SW
RP7
U16
U17
220
R17 220
C10 250pf
C6 250pf
C9 250pf
C5 250pf
C12 250pf
C8 250pf
C11 250pf
C7 250pf
RP6 330
R21 330
Q9 MJE251
Q5 MJE251
Q8 MJE251
Q4 MJE251
Q11 MJE251
Q7 MJE251
Q10 MJE251
Q6 MJE251
U16, U17, MPQ3725A
LOAD CLAMPS
LOAD CLAMPS
+5V
R24 470
CR5 IN4733
U3 TID121
U6 TID121
U5 TID139
U4 TID 139
RP2 10K
RP1 2K
R13 10K
R14 2K
CR3 IN4148
CR4 IN4148
J1
TP3
SP 48
SP 47
TP2
LOW RANGE LOADS
HIGH RANGE LOADS
TOLERANCES (EXCEPT AS NOTED)
DECIMAL ±
ANGULAR ±
DRAWN BY:
APPROVED BY:
DATA I/O ISSAQUAH WASH
TITLE SCHEMATIC DIAGRAM UniPak ADDRESS CARD
SIZE D
CODE IDENT NO
DRAWING NO. 008-1998
SCALE NONE
SHEET 2 OF 2


8
7
6
5
D
C
B
A
A0
A5
A1
A6
A2
A7
A3
A8
A4
A9
A10
A11
A12
A13
A14
A15
DO1
DI1
DO2
DI2
DO3
DI3
DO4
DI4
DO5
DI5
DO6
DI6
DO7
DI7
DO8
DI8
VER A
VER B
START
CLK INHIBIT
W/L
"26"
J1
J2,J3
P1
J1


4
3
2
1
REVISIONS
ZONE LTR DESCRIPTION OWN CK PE DATE
A RELEASE 1-80
B INCORP ADCH A1 PER ECP 0237 5/6/16
D
C
B
A
X
/VOH
20
Y
21
15 S
V
Z
OG
22
AA
16
23 26 DD
17 18 U V
RATE
BB
SE
24
EG H.V.
CC
E ENABLE
JJ
W
END
KK
30
25
31
CC
RAW
LL
T
32
25
MM
RLOCK
33
NN
RAW
34
D
PP
TE
35
RR
ET
36
J2, J3
EE
C4
Y
27
C1
21
FF
C5
Z
28
C2
22
HH
C6
AA
29
C3
23
P1
J2, J3
P/N 702-1999
APPROVALS
PROJ. ENG.
PROD. ENG.
CONF. MANG.
ENG. MGR.
DATE 1-17-80
TOLERANCES (EXCEPT AS NOTED)
DECIMAL
ANGULAR
DRAWN BY G. RYDER
CHECK
DATA I/O
TITLE SCHEMATIC DIAGRAM
MOTHERBOARD
SIZE D
CODE IDENT NO
DRAWING NO 008-1999
SCALE NA
SHEET 1 OF 1

U.S. Sales Offices and Representatives
Direct Sales and Service Offices

Data I/O Corporation
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
Telex Dom. 15-2167,
Int'l. 4740166 DIO UI

NORTHWEST REGION

Data I/O Corporation
1700 Wyatt Drive
Suite 1
Santa Clara, CA 95054
(408) 727-0641

SOUTHWEST REGION

Data I/O Corporation
2770 South Harbor Blvd.
Suite K
Santa Ana, CA 92704
(714) 662-1182 *(Sales)*
(714) 662-2498 *(Service)*
Telex 755870

EASTERN REGION

Data I/O Corporation
Nashua Road
Route 101A
Amherst, NH 03031
(603) 889-8511 *(Sales)*
(603) 889-8513 *(Service)*
Telex 943431

CENTRAL REGION

Data I/O Corporation
1810 N. Glenville Drive
Suite 108
Richardson, TX 75081
(214) 235-0044
Telex 792474

Representatives

ALASKA, WASHINGTON (TRI-CITIES, VANCOUVER), OREGON

Northwest Test and Measurement
8196 Southwest Hall
Suite 217
Beaverton, OR 97005
(503) 646-9966
1-800-247-5700
Telex 910-467-8775

WESTERN WASHINGTON, SPOKANE

Northwest Test and Measurement
4020 148th Ave. N.E.
Suite F
Redmond, WA 98052
(206) 881-8857

ARKANSAS, LOUISIANA, OKLAHOMA, TEXAS

TESTECH, Inc.
1000 E. Campbell Road
Suite 108
Richardson, TX 75081
(214) 644-5010

4800 West 34th St.
Suite D-6
Houston, TX 77092
(713) 956-0837

1715 Capital of Texas Hwy S.
Suite 107
Austin, TX 78746
(512) 327-7033

OHIO

Electro Sales Associates
1635 Mardon Drive
Dayton, OH 45432
(513) 426-5551

26250 Euclid Avenue
Suite 331
Cleveland, OH 44132
(216) 261-5440

MICHIGAN

Electro Sales Associates
29200 Vassar Road
Suite 505
Livonia, MI 48152
(313) 474-7320

9816 Portage Road
Portage, MI 49002
(616) 323-2416

PENNSYLVANIA, WEST VIRGINIA, EASTERN KENTUCKY

Electro Sales Associates
3740 Mount Royal Blvd.
Allison Park, PA 15101
(412) 487-3801

UPSTATE NEW YORK

DB Associates, Inc.
7000 E. Genesee Street
Building D
Fayetteville, NY 13066
(315) 446-0220

KANSAS, NEBRASKA

Midtec Associates, Inc.
7702 Mize Road
DeSoto, KS 66018
(913) 441-6565
Telex 910-743-4129

MISSOURI

Midtec Associates, Inc.
8460 Lindbergh North
Suite 11
Florissant, MO 63031
(314) 837-5200

FLORIDA

Pen Tech Associates
201 S.E. 15th Terrace
Suite K
Deerfield Beach, FL 33441
(305) 421-4989

1398 Semoran Blvd.
Suite 106
Casselberry, FL 32707
(305) 645-3444

GEORGIA, TENNESSEE

Pen Tech Associates
627 Cherokee Street
Suite 21
Marietta, GA 30060
(404) 424-1931

NORTHERN FLORIDA, ALABAMA, TENNESSEE, MISSISSIPPI

Pen Tech Associates
3322 Memorial Pkwy. S.W.
Suite 36
Huntsville, AL 35801
(205) 881-9298

NORTH CAROLINA, SOUTH CAROLINA

Pen Tech Associates
3709 Alliance Drive
Suite C
Greensboro, NC 27407
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MINNESOTA, NORTH DAKOTA, SOUTH DAKOTA

Torkelson Associates
4940 Viking Drive
Minneapolis, MN 55435
(612) 835-2414
Telex 910-576-2740

NORTHERN ILLINOIS, IOWA, INDIANA

Torkelson Associates
108 Wilmot Road, Suite 110
Deerfield, IL 60015
(312) 945-8700
Telex 910-992-1438

INDIANA, WESTERN KENTUCKY

Torkelson Associates
2346 S. Lynhurst
Room B101
Indianapolis, IN 46241
(317) 244-7867
Telex 810-341-3141

WISCONSIN

Torkelson Associates
2840 N. Brookfield Road
Brookfield, WI 53005
(414) 784-7736

ARIZONA, NEVADA

Zeus Electronics, Inc.
1428 E. Pierson Street
Phoenix, AZ 85014
(602) 263-6022
1-800-528-4512
Telex 910-951-1362

NEW MEXICO, EL PASO CO., TEXAS

Zeus Electronics, Inc.
8100 Mountain Road N.E.
Suite 111
Albuquerque, NM 87110
(505) 842-6633
1-800-528-4512

COLORADO, WYOMING

Zeus Electronics, Inc.
3333 Quebec Street
Suite 2950
Denver, CO 80207
(303) 321-4246
1-800-528-4512

UTAH, IDAHO, MONTANA

Zeus Electronics, Inc.
1849 W. North Temple
Suite B105
Salt Lake City, UT 84116
(801) 534-0500
(801) 534-0503

VIRGINIA, WASHINGTON D.C.

SCI-REP, Inc.
9512A Lee Highway
Fairfax, VA 22031
(703) 385-0600
Telex 710-833-0361

NEW JERSEY, EASTERN PENNSYLVANIA

SCI-REP, Inc.
304 Cooper Center
Pennsauken, NJ 08109
(609) 662-5222
Telex 710-892-1297 SCI-REP PESN

Addresses on this list subject to change without notice.

0321/784

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Data I/O Europe
Vondelstraat 50-52
NL-1054 GE Amsterdam
The Netherlands
(20)186855
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